OPERATING INSTRUCTIONS

Test Set

Q-14404

1.00

TYPE 1392-A

TIME-DELAY GENERATOR

SERIAL #248

DEPT. 816

1392-A

GENERAL RADIO COMPANY

OPERATING INSTRUCTIONS

TYPE 1392-A

TIME-DELAY GENERATOR

Form 1392-0100-C
February, 1961

GENERAL RADIO COMPANY
WEST CONCORD, MASSACHUSETTS, USA

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SPECIFICATIONS

INPUT SYSTEM

Voltage:
Sine Wave, 0.1 volts rms.
Square Wave, 0.3 volt, peak-to-peak.
Pulse (negative or positive), 1 volt peak ac or dc, input trigger threshold control provided.

Frequency: dc to over 300 kc.

Time Delay (Input to direct sync): 0.12 ± 0.02 μsec.

Direct Sync Pulse:
Amplitude, 15 volts or more, positive or negative.
Duration, 0.13 ± 0.02 μsec.
Impedance, 93 ohms or less.

DELAY NO. 1

Delay Range: 0–1.1 sec in seven ranges.

Accuracy: 1 μsec–1.1 sec range, ±1% of dial reading; 0–1 μsec range, ±0.01 μsec.

Stability: Jitter, 1:30,000 at worst.
Drift, 1:10,000 with 20% line variations.

Resolution: 0–1 μsec 0.004 μsec.
1 μ sec–1 sec 1:8800.

Duty Ratio Effects: Less than dial accuracy to 60% 5% at duty ratio of 80%.

DELAY NO. 1 SYNC

Duration: 0.1 ± .02 μsec.

Amplitude: 25 volts or more positive or negative.

Impedance: 93 ohm output impedance
Monitor Lamp NE-2.

Max PRF: 0–1 μsec range, 300 kc;
1 μsec–1.1 sec range, 250 kc (at 1 μsec).

DELAY NO. 2, OR COINCIDENCE CIRCUIT

Range: 0.5 μsec–0.5 sec (six decade ranges).

Accuracy: ±3% of dial reading.

Stability: Jitter, 1:20,000.
Line Drift, 1:5,000 for 20% line change.

Resolution: 1:2,000.

Delay No. 2 Sync:
0.13 μsec ± 0.02 μsec.
20 volts or more, positive or negative.
93 ohms.
Monitor Lamp.

Duty Ratio Effects: Full scale, less than dial accuracy at 60% duty ratio; bottom of scale, less than dial accuracy at 20% duty ratio. Max. PRF 300 kc.

Coincidence:
Input, positive or negative pulse, 5 volts or over.
Input frequency, 1 cps to 1.7 Mc (for single pulse selection).
Input pulse rise time, 0.1 μsec or less at 5 v.

Power Supply: 105 to 125 (or 210 to 250) volts, 50–60 cycles, 180 watts at 115 volts. Power receptacle will accept either 2-wire (TYPE CAP-35) or 3-wire (TYPE CAP-15) Power Cord. Two-wire cord supplied.

Dimensions: Panel, 19 × 8¾ inches; depth behind panel, 13 inches.*

Accessories Supplied: TYPE CAP-35 Power Cord; spare fuses; test lead; 4 TYPE 874-C58 Cable Connectors.

Net Weight: 35 pounds. **

* (485 by 225 by 330 mm.)

**(16.0 kg.)

U.S. Patent No. 2,548,457.

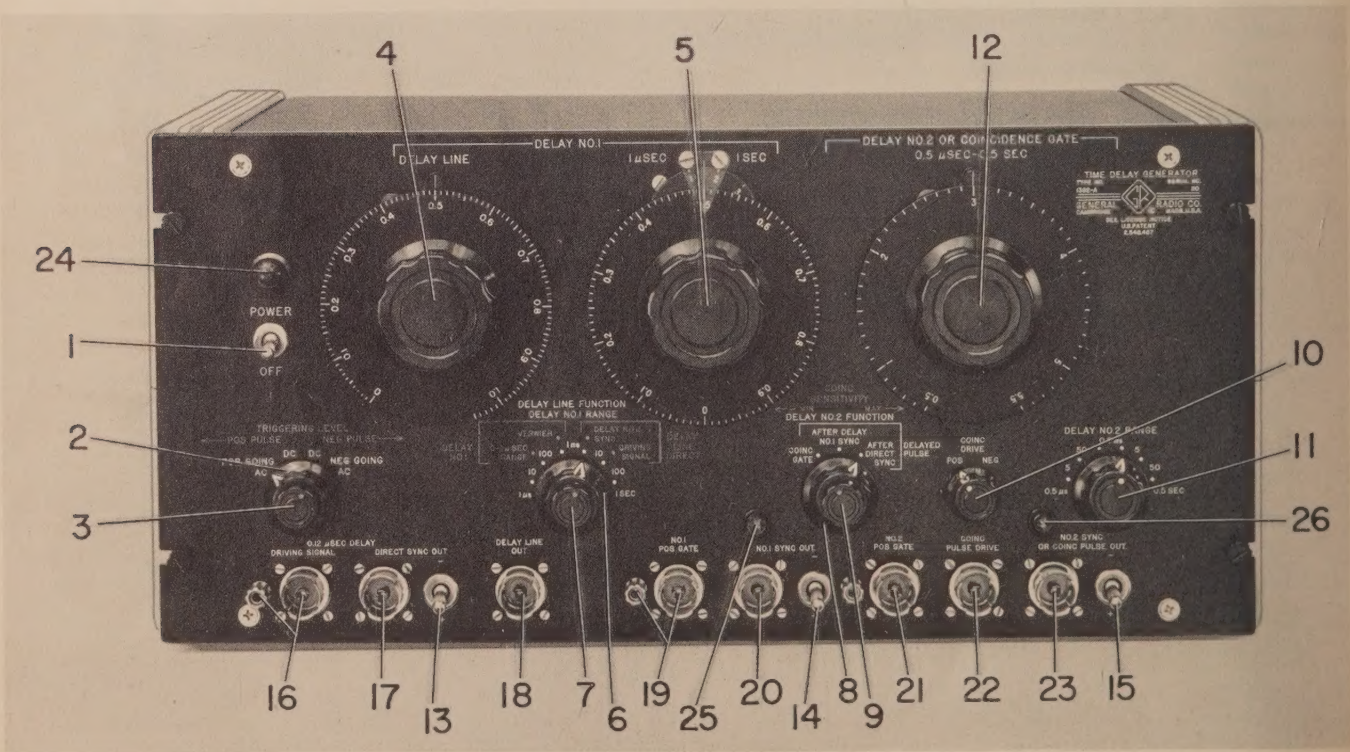

Figure 1.1. Type 1392-A Time-Delay Generator.
(Refer to paragraph 1.3 for legend.)

TYPE 1392-A
TIME-DELAY GENERATOR

Section 1
INTRODUCTION

1.1 PURPOSE. The Type 1392-A Time-Delay Generator (Figure 1.1) is a general-purpose instrument designed to produce accurately controlled stable pulses to indicate time intervals between a time reference signal (generated either by an outside source or within the instrument itself) and output signals. These pulses, of 0.1-μsec duration, are adjustable in time to produce intervals that can be set by controls direct-reading in time units.

Gate signals, which start and stop at times coincident with the marker pulses, provide steps at the limits of the delay intervals; these steps are more easily displayed on the cathode-ray screen than are the brief marker pulses. One of these gate signals also makes possible the selection and display of external signals occurring during preselected time intervals.

Signals to modulate the main time-delay circuit can be applied to produce pulse-duration or pulse-position modulation.

1.2 DESCRIPTION. The Type 1392-A Time-Delay Generator produces a precisely controlled delay direct-reading in time between an internally formed reference pulse and secondary, similarly shaped pulses. It effects this delay either by delaying the reference pulse in a 0-1-μsec variable delay line, or by producing the delay with a linear ramp function of controlled slope whose amplitude is compared with a dc voltage established by the setting of the time-delay control dials. This latter method is used to produce a main (No. 1) delay of 1 μsec to 1 second and a secondary (No. 2) delay of 0.5 μsec to 0.5 second. Both main and secondary delay circuits are in six decade ranges, with linear dials.

It is not possible to produce an accurate, stable, and linear delay of high resolution down to zero with the ramp and reference system used for the main and secondary delays mentioned above, so the variable delay line is used to produce a delay of 0 to 1 μsec relative to the reference synchronizing pulse, and the range of the main delay circuit is thereby extended down to zero.

A versatile input circuit is provided so that the time-reference synchronizing pulse can be produced from almost any shape of input signal and over a wide range of input voltages and frequencies.

1.3 CONTROLS AND CONNECTORS. The following tables list controls, connectors, and indicators on the front panel of the Type 1392-A:

TABLE OF CONTROLS

FIG. 1.1 REF	NAME	TYPE	FUNCTION
1	POWER	Toggle switch	Turns instrument on or off.
2	Input Selector (not labeled on front panel)	4-position rotary switch	Selects direction of zero crossing to trigger DIRECT SYNC signal. Also removes or inserts blocking capacitor at input.

TABLE OF CONTROLS (CONT)

FIG. 1.1 REF	NAME	TYPE	FUNCTION
3	TRIGGERING LEVEL	Continuous rotary control (Concentric with Input Selector)	Sets correct level for operation from input signals of various types and amplitudes. Allows DIRECT SYNC to be set to occur exactly at zero crossing.
4	DELAY LINE	Continuous rotary control and dial	Delay line setting.
5	1 μSEC - 1 SEC	Continuous 10-turn rotary control and dials	In conjunction with DELAY No. 1 RANGE switch, sets delay interval between direct sync and Delay No. 1 sync.
6	DELAY LINE FUNCTION	4-position rotary switch	Selects function of delay line in circuit system.
7	DELAY No. 1 RANGE	6-position rotary switch (Concentric with DELAY LINE FUNCTION)	Selects operating range of Delay No. 1 control.
8	DELAY No. 2 FUNCTION	3-position rotary switch	Selects operating function of Delay No. 2 as coincidence circuit or as a delay, and selects initiating time of delay.
9	COINC SENSITIVITY	Continuous rotary control (Concentric with DELAY No. 2 FUNCTION)	In coincidence operation, sets threshold level at which external coincidence signal will trigger delayed sync. In delay functions determines amplitude of No. 2 gate.
10	COINC DRIVE	2-position rotary switch	Sets coincidence circuit for operation from coincidence input of either polarity.
11	DELAY No. 2 RANGE	6-position rotary switch	Selects operating range of DELAY No. 2 or COINCIDENCE GATE.
12	DELAY No. 2 OR COINCIDENCE GATE	Continuous rotary control and dial	In conjunction with DELAY No. 2 RANGE switch, determines Delay No. 2 of coincidence gate interval.
13	DIRECT SYNC OUT	Toggle switch	Selects polarity of direct sync signal output.
14	No. 1 SYNC OUT	Toggle switch	Selects polarity of No. 1 sync signal output.
15	No. 2 SYNC OR COINC PULSE OUT	Toggle switch	Selects polarity of No. 2 sync or coincidence pulse output.

TABLE OF CONNECTORS

FIG. 1.1 REF	NAME	TYPE	FUNCTION
16	DRIVING SIGNAL	Type 874 Connector and binding post	Input to instrument for prf-determining signal.
17	DIRECT SYNC OUT	Type 874 Connector	Output of direct sync for reference.

Note that when the gate starting time is moved beyond 60 or to less than 50 μsec the sync pulse is lost. Now repeat this experiment after increasing the COINCIDENCE GATE duration controls for a gate lasting 12 μsec. Note now that either one or two coincidence drive pulses will be selected. Longer gates will admit more pulses.

The foregoing illustrates the general principles and operation of the coincidence circuits. The limits of operation in frequency and input voltage may now be established if the coincidence driving pulse amplitude and frequency are varied. Reduce the coincidence gate duration to 0.5 μsec. Apply a 1-Mc pulse train to the COINC PULSE DRIVE terminals, and attempt to select individual 1-μsec pulses. If, after careful adjustment of the COINC SENSITIVITY control, it is not possible to select an individual 1-μsec pulse without the "leading edge" of the gate itself forming a sync pulse, then the amplitude of the 1-μsec driving pulses is inadequate (refer to Specifications). In this instance, or for that matter whenever the driving pulse amplitude is marginally low, the maximum possible coincidence sensitivity can be obtained by means of a short circuit placed on the No. 2 POS GATE terminals. Naturally, the usual monitor provided at these terminals will be lost, so amplification of the driving pulses is preferable if the equipment is available.

Since the coincidence gate can be reduced sufficiently in duration to permit selecting 1-μsec pulse periods, provision has been made to delay the No. 2 sync or coincidence pulse by means of the 0-1-μsec delay line interval. Set the DELAY LINE FUNCTION switch to DELAY No. 2 SYNC. Observe the Delay No. 2 sync pulse and then the pulse at the DELAY LINE OUT terminals as the DELAY LINE setting is varied from 0 to 1 μsec. In this function there is no electronic sync signal generator following the delay line, so some baseline ripples, pulse broadening, and amplitude decrease with increasing delay will be seen. These same effects will be found when a driving signal is passed through the line with the DELAY LINE FUNCTION switch in the DRIVING SIGNAL position.

Section 3

CIRCUIT DESCRIPTIONS

3.1 GENERAL. This section contains a sufficiently detailed description of the functioning of the individual circuits and components of the Type 1392-A Time-Delay Generator to enable the technician to service and calibrate the instrument with confidence. In general, the organization of this section will follow signal flow through the instrument, and reference will not be made to specific voltages, gains, etc. These data will be found in Section 5. Before reading or attempting to use this section, reread paragraph 1.5 for familiarization with the switching. The circuit diagrams fold out at the rear of this manual so that the individual circuits discussed in this and subsequent sections can be followed. For the sake of brevity, the action of the more common pulse circuits, Schmitt trigger, bistable, and blocking oscillator cannot be discussed in detail. Complete details about these circuits can be found in standard reference works.[1]

3.2 INPUT CIRCUITS.

3.2.1 GENERAL. Refer to the schematic diagram, Figure 5.5. The block diagram shows that this circuit system consists of three tubes which accept the input driving signal at J101, process it to form the direct sync pulse at J102, and provide a triggering signal for the other circuits in the instrument. These circuits permit control of the following input-signal characteristics by the operator:

a. He can select whether the input signal is a-c or d-c coupled to the trigger-generating circuits.

b. He can select whether a negative-going or positive-going slope of the input signal will cause the sync signal to be formed.

c. He can set, within a limited range, the d-c level at which the sync signal is formed. This operation is more complex than first appearances indicate, since by means of the TRIGGERING LEVEL control, the input sensitivity can be optimized for pulses of either polarity or for sine or square waves. When the latter waveforms have an amplitude greater than the minimum value, this control can be used to establish the direct sync pulse upon either zero-crossing of an input waveform.

3.2.2 AMPLIFIER, LIMITER AND SCHMITT TRIGGER CIRCUITS. Let us now follow a signal through these circuits. A signal applied at J101 is coupled either directly or via C101 to the grid of the input d-c amplifier, V101, through a limiter consisting

[1] E.g.: Millman and Taub, Pulse and Digital Circuits, McGraw-Hill, N.Y., 1956.

of silicon diodes D101 and D102. If there is a d-c component in the input signal, the input selector switch should be set on AC to prevent saturation of V101 and the limiter. The limiter is present to prevent shifts in the triggering level with higher input amplitudes. D-c coupling is provided expressly to permit triggering of the instrument on slowly varying signal voltages. The plate of the input amplifier (pin 1, V101) is directly connected to the input grid, (pin 2, V102) of a Schmitt trigger circuit.[2] The quiescent plate current of V101 sets the grid voltage of this circuit at a value near to that corresponding to the center of its hysteresis range. The exact value of this quiescent voltage is determined by R106, the TRIGGERING LEVEL control. For optimum sensitivity, R106 should be set to produce at pin 2 of V102 a grid voltage in the center of the hysteresis region. For positive pulses, the input is below the hysteresis region, and for negative pulses it is above the hysteresis region.

Assume now that a sinusoidal signal is applied at the DRIVING SIGNAL terminal. As the signal swings from negative to positive, the amplified signal at the plate of V101 swings the grid of V102 negative. V102 will switch so that the left-hand side goes off and the right-hand side comes on. If S101 is set for POS GOING drive, the positive transition of the left-hand side of V101 is coupled through contacts 101R and 112R to the grid (pin 2) of V101 via the differentiating circuit, C104 and R112. For negative-going drive, the opposite plate of the Schmitt circuit is selected by S101.

3.2.3 DIRECT TRIGGER GENERATOR AND BLOCKING OSCILLATOR CIRCUITS. The pulse-forming amplifier consisting of the pentode section of V101 is normally held in cutoff by fixed bias established by R112 and R113. It is turned on briefly when the Schmitt circuit switches. The pulse of plate current in this tube is drawn through winding 3-5 of T101, and induces a positive voltage at the grid (pin 3) of the blocking oscillator, V103.[3] This positive voltage removes a sufficient amount of bias to cause the oscillator to start. This bias is set by R128, R122, and R123. Note that the value of R128 may vary from one instrument to the next. It is chosen during calibration to produce a grid bias of -18.5 volts in the face of variation in the Thyrite units. The pulse of plate current in the blocking oscillator produces the negative direct trigger across R118 and the positive direct sync pulse coupled through the delay network L101, C107 to the grid (pin 8) of the output tube, V103. The positive direct sync pulse is produced across R124, and the negative pulse across R119. Sync output polarity is selected by S102.

3.2.4 DELAY LINE SWITCHING. The direct trigger is coupled to contact 101R of S301 to start the Delay No. 2 circuits in the AFTER DIRECT SYNC position of the DELAY No. 2 FUNCTION switch, and is also coupled to contact 103R of S202. S202 is the DELAY LINE FUNCTION switch, which determines whether the delay line triggers the Delay No. 1 sync-generating blocking oscillator in the 0-1-μSEC RANGE or simply delays the direct trigger by up to 1 μsec (the VERNIER position). Note that when the DELAY LINE FUNCTION switch is set in either DELAY LINE DIRECT position, the direct trigger is passed directly to V201 via contacts 103R and 105R to start the Delay No. 1 circuits. In this way, the Delay No. 1 circuit functions normally when the delay line is used for other purposes.

Inputs to the delay line in the two DELAY LINE DIRECT positions are through switch contact 112R of S202 for the DELAY No. 2 SYNC position, and contact 102R for the DRIVING SIGNAL position. Note that, in the DRIVING SIGNAL position, any d-c component in the input signal is blocked by C111. For the various positions of the DELAY LINE FUNCTION switch, S202, proper input and output terminating impedances are afforded by R215, R126, R131, and R132. These resistors are shown in Figure 5.5 with nominal values. They may be changed in instrument calibration to slightly different values to optimize performance with variations from one delay line to the next.

3.3 DELAY NO. 1 CIRCUITS. (See Figure 5.6.)

3.3.1 GENERAL. The action of the electronic circuits to produce the 1-μsec to 1-second Delay No. 1 sync is started by the direct trigger pulse from S202 applied via C204 to pin 2 of V202 to open the Delay No. 1 gate. When the gate is opened, the sweep generator, V203, is started. The slope of the sweep produced by this stage and by V204 is determined by R-C elements selected by the DELAY No. 1 RANGE switch, S201. When the sweep voltage rises to equal the reference voltage established by the 1-μSEC - 1-SEC control, the amplitude comparator (V205, V208, and V211) switches. The switching of the amplitude comparator produces a positive pulse, amplified in V206 and used to start the Delay No. 1 blocking oscillator, V207. The pulse of current in V207 sets the gate bistable to its off position, resets the sweep by turning V203 on, and ends the delay interval. Note that in the 0-1-μsec range, the delay line output is fed directly to V206 to start the blocking oscillator.

3.3.2 DELAY NO. 1 GATE. V201, the Delay No. 1 gate tube, is a bistable circuit.[4] The left-hand half of V201 is normally "on" and the high plate

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[2]Ibid, p. 164.

[3]Ibid, p. 282.

[4]Ibid, p. 140.

voltage (+150 volts) on the right-hand half keeps the grid (pin 2) of V203 positive with respect to ground and holds this tube in the "on" state. The cross-coupling network (R212 and R210) from the right-hand plate to the left-hand grid will permanently hold V201-left "on". Note that D202 and D203 are negative grid clamps that prevent the "off" grid of V201 from being more than 12 volts negative. The negative direct trigger pulse coupled through C204 and D201 will turn V201-left off and V201-right on. The resulting negative voltage at pin 2 of V203 will turn the sweep generator off and start a delay interval.

3.3.3 DELAY NO. 1 GATE AMPLIFIER. V202, the gate amplifier, is directly coupled to the left-hand plate of the gate through R205 and R206. When a delay interval is started, the rise in voltage at its grid causes its plate current to increase. A positive pulse is produced in R201 and a negative pulse at R202. The positive "gate" pulse is fed to J201 on the front panel and the negative pulse to J204 on the rear panel. Note that J204 is fed through C201, and hence is not capable of remaining flat over long-time intervals when a d-c load impedance is connected at J204.

3.3.4 DELAY NO. 1 SWEEP GENERATOR. V203 and V204 and their associated components comprise the circuit that produces the positive ramp establishing the Delay No. 1 interval. When the gate is triggered, pin 2 of V203 is driven negative with respect to ground. The slope of its rising plate voltage is set by the R-C network selected by S201, the DELAY No. 1 RANGE switch. The positive-going plate voltage of V203 is fed to pin 1 of V204, the bootstrap cathode follower. The rising cathode voltage at pin 3 of V204, coupled through C216, turns D205 off. The gain of this cathode follower is nearly unity, and the voltage at the top end of the sweep time-constant resistors is therefore nearly equal to that at the bottom ends. Thus, the current available to charge the sweep capacitors is nearly constant, and a linearly rising ramp is produced. The gain of the cathode follower, V204, is increased by a large cathode resistor, R236. When the delay interval is ended, this voltage must be rapidly returned to a low value. Fast reset is accomplished by the other half of V204, which is "off" during the active interval and is turned on by the gate coupled through R234 and C221 at the end of the active interval.

The reference time constant establishing the sweep slope is that of R225 and C212 (10-100-msec range). The slopes of all other ranges are adjusted to agree with this one during instrument calibration by means of the various range-calibrating potentiometers. In the 1-10-μsec range, some of the positive voltage from the gate bistable is inserted by C215 to establish the minimum delay accurately. C212 is used both on the 10-100-msec range and on the 100-msec-to-1-second range. In the 100-msec-to-1-second range the time constant is increased by a decade by increasing resistance (R226). A "step" must be inserted in this sweep to compensate for the reduced plate voltage on V203. This step is produced across R231, the 100-msec adjustment.

3.3.5 AMPLITUDE COMPARATOR. The rising sweep ramp is coupled to the grid (pin 7) of V208 in the amplitude comparator circuit. When the ramp rises to equal the voltage set by the 1-μsec-to-1-second control at pin 2, the circuit switches and resets the sweep. This equality is established by the amplitude comparator. Normally, with V203 conducting, the voltage at pin 7 will be less than that at pin 2, and the left-hand side will be "off". V205 can be compared to a bistable in which the normal grid-ground resistors of the cross-coupling networks are replaced by the plate resistance of V208. If the grid voltage at pin 7 is slowly increased so that it is just equal to that at pin 2, the circuit will still be stable with equal current in both halves of V208. Any increase in the voltage at pin 7 beyond this point will be amplified by this half of V208, and when the bias on V205-left has decreased sufficiently, V205 switches in a regenerative fashion with the left-hand half going "off" and the right-hand half turning "on". The positive pulse generated at the plate (pin 6) of the left-hand half of V205 produces the Delay No. 1 reset trigger.

The Delay No. 1 sweep voltage varies from about 10 to 110 volts with respect to ground over its control range. The voltages at the grids of V208 must follow this variation. V211 permits this voltage variation at the grids of V208 by establishing a constant current irrespective of voltage.

3.3.6 RESET TRIGGER GENERATOR, DELAY NO. 1 BLOCKING OSCILLATOR, AND INDICATOR CIRCUITS. The right-hand section of V206 is turned on by the positive pulse from the amplitude comparator and triggers the Delay No. 1 blocking oscillator. This circuit is identical in function and configuration to that of V102 and V103 in the input circuits (refer to paragraph 3.2). The pulse of plate current of V207-right develops a negative pulse across R244. This pulse is coupled through C209 and D204 to reset the gate bistable.

The positive Delay No. 1 sync pulse is used to turn V206-left off to light the indicator lamp V209. This positive pulse is coupled through capacitor C229, and causes the grid to draw current. This current charges C229, which discharges through R267, developing a negative voltage. This "grid-leak" bias voltage turns the tube off and causes its plate voltage to rise sufficiently to ionize V209. A single pulse will cause ionization and will register as a brief flash of light.

3.3.7 SWEEP REFERENCE VOLTAGE, SWEEP CLAMP, TIME-MODULATION INPUT CIRCUITS. The Delay No. 1 reference voltage corresponding to the setting of the 10-turn 1-μSEC - 1-SEC control, R262, is established by a voltage divider between 250 volts regulated and ground. R261 (Delay No. 1 minimum) and R263 (Delay No. 1 maximum) are used to set voltages corresponding to 10-msec and 100-msec delays respectively. The voltage established at the junction of R219 and R268 on the "ground" end of this voltage divider is applied to pin 6 of V203, the sweep clamp. When the sweep generator is conducting in the quiescent portion of the cycle, this diode conducts and stabilizes the quiescent value of the sweep voltages. Variations in plate resistance of the sweep generator tube from one tube to the next and with age are thereby minimized by both clamping action and feedback to the reference voltage divider.

Voltage from the time modulation jack (J203) is coupled in through C228 and developed across R260. Note that J203 is a short-circuiting jack. C228 is normally grounded to reduce noise at the grid (pin 2) of V208 and to minimize jitter. If it is desired to control Delay No. 1 with an external d-c signal, C228 can simply be shorted out and J208 permanently held open (or a plug-in C228 can be constructed to be used when no external signal is inserted).

3.3.8 AUTOMATIC RESET CIRCUIT. Since the delay gate is a bistable circuit, it must always receive a reset pulse to terminate the delay interval. Several conditions can arise that will disable this natural reset pulse momentarily. Once the amplitude comparator has fired and the gate bistable has failed to reset, the sweep will stay "up", and the circuit will be stable in this "locked-out" condition. An automatic resetting circuit (R259, C226, V210) provides a positive pulse at the grid of the gate bistable. This pulse will reset the circuit if the sweep is "up" for much more than a second. Under any normal circumstances the average voltage on C226 is too low to ionize V210, but on failure this voltage rises to 120 volts or more and V210 ionizes, resetting the gate.

3.4 DELAY NO. 2 AND COINCIDENCE CIRCUITS. (See Figure 5.7.)

3.4.1 GENERAL. The delay time interval is produced by circuits having configuration identical to those of Delay No. 1. The only differences are that the sweep generator and amplitude comparator are simplified and the triggering and output circuit configurations are different to accomodate the coincidence operation and to permit Delay No. 2 to be started after the Delay No. 1 interval.

In the block diagram, the three positions of the DELAY No. 2 FUNCTION switch are COINC GATE, AFTER DELAY No. 1 SYNC, and AFTER DIRECT SYNC, hereafter referred to as positions 1, 2, and 3, respectively. Note that the circuit connections to V303, the reset trigger generator, and to V306, the Delay No. 2 blocking oscillator, are the same in positions 2 and 3. In these two positions, only the input trigger pulse is changed, and the sync pulse is formed after the delay interval established by the sweep and amplitude comparator, as in the Delay No. 1 circuits. In positions 2 and 3, V303-right drives V306 to form the reset pulse for the gate and an output sync pulse.

In position 1, the COINC GATE setting of the switch, the Delay No. 2 gate is opened by the Delay No. 1 trigger pulse, but V303-right resets the gate directly to terminate the delay interval. The Delay No. 2 blocking oscillator is driven from the coincidence amplifier stage. In this stage the Delay No. 2 gate and the output of the coincidence pulse-amplifier stage are additively applied. Only a proper combination of these two signals will trigger the blocking oscillator to produce a sync pulse.

3.4.2 DELAY NO. 2 GATE. V301, the Delay No. 2 gate, is a bistable identical to that described in paragraph 3.3.2, in which the left-hand side is normally "on" and the right-hand side "off". The right-hand-side plate voltage is high (+150 volts) and the sweep generator (V302-left) is conducting at zero bias holding the sweep at a low, quiescent value of voltage. The negative trigger from either input circuits or Delay No. 1 circuits is applied through C301 and D301 to start the delay interval by turning V301-left off.

3.4.3 DELAY NO. 2 SWEEP CIRCUIT. When V302-left is in its quiescent state, it is "on" in zero bias, with a plate voltage less than 12 volts. V302-right acts as a clamp on this voltage by conducting when its cathode voltage is less than that across R315. This voltage is set by the current in the reference voltage divider made up of R330, R331, R332, R333, and R315. The clamping action stabilizes the quiescent conducting voltage and refers it to the reference voltage supplied to the amplitude comparator Schmitt circuit, V304. The time constant for each range is not individually adjusted; R317 is adjusted for the compromise in accuracy compared with the 500-msec-to-0.5-second-range time established by R319 and C307. Note that "steps" (R321 and R322) are provided in the two fastest sweeps for overcoming the effects of stray capacitance, and that C313 is provided to adjust the minimum end of the 0.5-μsec-to-5-μsec range.

3.4.4 AMPLITUDE COMPARATOR. V304, the Delay No. 2 amplitude comparator, is a Schmitt trigger circuit. The cathode voltage is set by the 0.5-

therefore, the delay line is simply connected between the DRIVING SIGNAL terminals and the DELAY LINE OUT terminals and functions as a passive device. In this connection the electronic portions of the instrument are still operative, but the high-frequency input impedance is now that of the delay line (approximately 250 ohms).

1.5.4 DELAY NO. 1 (ELECTRONIC). The electronic portions of the Delay No. 1 circuit system are not operative when the DELAY LINE FUNCTION switch is set in the 0-1-μSEC RANGE position. In the other three positions of this switch the electronic delay circuits operate to produce the No. 1 POS GATE and the No. 1 SYNC OUT. With the DELAY LINE FUNCTION switch in either the DELAY No. 2 SYNC or DRIVING SIGNAL position, these circuits produce a calibrated delay of 1 μsec to 1 second between the DIRECT SYNC OUT and No. 1 SYNC OUT terminals.

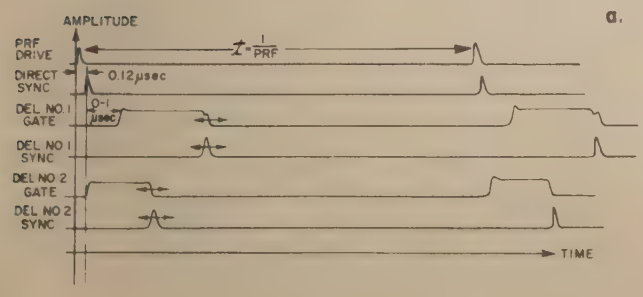
The No. 1 delay circuit consists of a bistable multivibrator, linear sweep generator, amplitude comparator, and reset trigger-forming circuits which drive the No. 1 sync-blocking oscillator. The bistable multivibrator is set to start the delay interval by the direct trigger (or delay line output in VERNIER position). The bistable multivibrator controls the linear sweep generator, which produces a ramp whose slope is set by the DELAY No. 1 RANGE switch in decades. This sweep voltage rises to a value determined by the setting of the 1-μSEC - 1-SEC control. When these two voltages are equal, the amplitude comparator fires, produces the Delay No. 1 sync, and resets the bistable multivibrator to its quiescent condition.

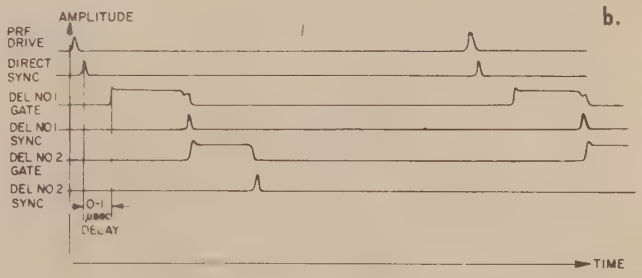
1.5.5 DELAY NO. 2 AND COINCIDENCE CIRCUITS. The circuits of Delay No. 2 are identical in principle to those of Delay No. 1 just described. The Delay No. 2 interval of 0.5 μsec to 0.5 second is started by the control bistable multivibrator set with either the direct trigger pulse or the Delay No. 1 trigger pulse. The Delay No. 2 control settings read the time of formation of the No. 2 sync pulse after the DIRECT SYNC pulse or after the No. 1 sync pulse, depending on whether the direct trigger or Delay No. 1 trigger pulse was used. These two modes of operation correspond to the AFTER DIRECT SYNC and the AFTER DELAY No. 1 SYNC settings of the DELAY No. 2 FUNCTION switch, respectively (see Figures 1.3a and 1.3b). When this switch is set in the COINC GATE position, the No. 2 bistable multivibrator is set to start the delay action by the Delay No. 1 trigger, and a gate corresponding in duration to the setting of the No. 2 delay controls is produced (see Figure 1.3c). The No. 2 sync pulse will now be produced only upon proper setting of the COINC SENSITIVITY control and upon the introduction of a pulse at the COINC PULSE DRIVE terminals. The operation of the Delay No. 1 circuit, the No. 2 delay-gate circuit, and coincidence pulse drive for time selection is shown in Figure 1.4. The presence of the No. 2 gate simultaneous with a coincidence driving pulse is necessary to produce a Delay No. 2 sync pulse. If the Delay No. 2 gate exists for an interval less than the interval between two successive driving pulses, only one pulse will be selected. If it "brackets" more than one pulse, then all pulses so "bracketed" will be selected. This system permits steps of delay as precisely controlled as the

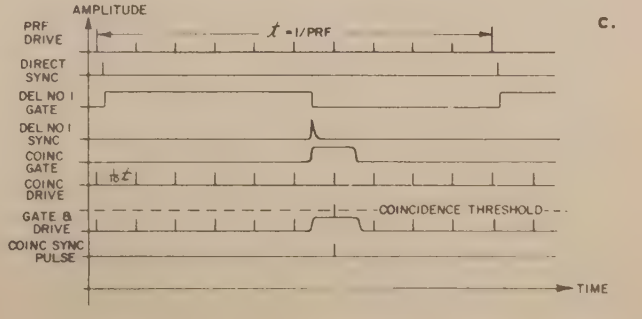
Figure 1.3a. Time-Sequence Diagram (DELAY LINE FUNCTION Switch at VERNIER, DELAY No. 2 FUNCTION Switch at AFTER DIRECT SYNC).

Figure 1.3b. Time-Sequence Diagram (DELAY LINE FUNCTION Switch at VERNIER, DELAY No. 2 FUNCTION Switch at AFTER DELAY No. 1 SYNC).

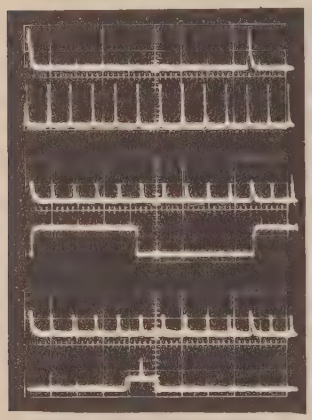
Figure 1.3c. Time-Sequence Diagram, Coincidence Operation.







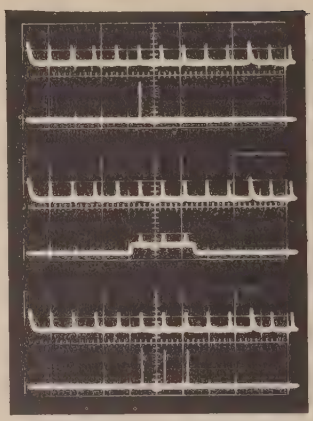
interval between coincidence driving pulses, reduction of jitter to that existing between the instrument driving signal and the selected coincidence driving signal, and the production of bursts of Delay No. 2 sync pulses.



(a)
100μs Timing pulses (to PRF drive)
10μs Timing pulses (to COINC drive)

(b)
10μsec and 100μsec timing pulses
Delay No. 1 GATE, $\simeq$ 48μsec

(c)
Combined time markers
COINC GATE, showing selected pulse. Delay No. 1, 45μsec; Delay No. 2, $\simeq$ 10μsec



(d)
Timing markers with COINC pulse at 50μsec

(e)
Delay No. 2 GATE, $\simeq$ 30μsec (Note selected pulses showing.)

(f)
Delay No. 2 SYNC pulses at 50μsec, 60μsec, 70μsec

Figure 1.4. Coincidence Circuit Used For Multiple Pulses.

Section 2

OPERATING PROCEDURE

2.1 GENERAL. In this section instructions will be given first for a general survey of the operation of the Time-Delay Generator, and second for the individual functions of the instrument.

The following is a list of auxiliary equipment necessary for a complete checkout of the instrument operation:

a. PRF Driving Sources

(1) Test Oscillator: RC or beat oscillator capable of operation from 20 cycles or less to 500 kc. General Radio Type 1210-C is recommended.

(2) Timing Pulse Generator: A source of time-coherent pulses is necessary to study the coincidence system. Tektronix Type 180-A or equivalent is recommended.

b. Oscilloscope to observe the delay intervals and marker pulses

It is convenient to have a dual-channel oscilloscope in order to observe the time relationships of the various marker pulses and gates relative to the direct sync pulse. In addition, the oscilloscope used should have at least 20-mμsec vertical rise time capability if the shape of the sync pulses is to be accurately observed. A satisfactory oscilloscope is the Tektronix 541, 543, or 545 with a dual-channel plug-in unit (53-54-C) or equivalent.

2.2 BASIC CONTROL SETTINGS. The following are the initial settings for the instrument controls:

POWER	On
Input Selector	POS GOING AC
TRIGGERING LEVEL	Midsetting
DIRECT SYNC OUT	+
DELAY LINE	0
DELAY LINE FUNCTION	Vernier
DELAY No. 1 RANGE	1 - 10 μs
1 μSEC - 1 SEC	5.0
No. 1 SYNC OUT	+
DELAY No. 2 FUNCTION	AFTER DIRECT SYNC
COINC SENSITIVITY	Fully clockwise
COINC DRIVE	POS
DELAY No. 2 RANGE	5 - 50 μs
0.5 μSEC - 0.5 SEC	0.5
No. 2 SYNC or COINC PULSE OUT	+

2.3 INITIAL OPERATION. Make certain that fuses and air filter are in place, and that the fan turns freely. Connect the Type 1392-A to a source of proper voltage and frequency as indicated on the nameplate near the power connector. Turn the POWER switch on. The pilot light above the switch should light. Set controls to the positions listed in paragraph 2.2.

Connect the signal generator to the DRIVING SIGNAL terminal, applying a 10-kc signal of about 1 volt rms. After the instrument has warmed up, both the Delay No. 1 and Delay No. 2 neon monitor bulbs on the front panel should light. If they do not, turn the TRIGGERING LEVEL control further until they do.

Connect the vertical input of the oscilloscope to the DRIVING SIGNAL terminal. Set the oscilloscope for internal triggering and set the triggering level and time base to display about 5 cycles of the input signal. Transfer the oscilloscope input to the DIRECT SYNC OUT terminal. Adjust the oscilloscope triggering if necessary and observe a train of 20-volt, 0.1-μsec pulses, one for each cycle of the input signal. This is the direct sync signal, which is the time reference for the instrument. Connect the oscilloscope trigger input to the DIRECT SYNC OUT terminal, and set the oscilloscope controls for external triggering so that other signals observed will appear in time relation to this reference.

Move the vertical input probe to the No. 1 POS GATE terminal, and set the DELAY No. 1 RANGE selector to 10-100 μsec. Several 5-μsec gate pulses should be observed, each starting with the direct sync and having a duration as indicated by the setting of the DELAY No. 1 RANGE and 1-μsec - 1 second controls. Vary these controls and note the effect on the gate signal; especially note erratic behavior and countdown as the delay time exceeds 80%-90% of the 100-μsec period established by the 10-kc driving signal.

With the DELAY No. 1 set for 20 μsec, move the oscilloscope probe to the No. 1 SYNC OUT terminal. Sync pulses about 25 volts in amplitude and occurring at the end of each gate pulse will be observed.

Restore the DELAY No. 1 controls to their basic settings (paragraph 2.2), move the oscilloscope probe to No. 2 POS GATE terminal and turn the COINC SENSITIVITY control fully clockwise. A gate signal, initiated at the time of the direct sync, whose duration is determined by the DELAY No. 2 RANGE and 0.5-μSEC - 0.5 SEC controls, will be observed. Note the effect of these controls on the gate.

With the DELAY No. 1 again set for about 20 μsec, move the probe to the No. 2 SYNC OUT terminal and observe the 25-volt sync pulse occurring at the end of the gate. The delay of these sync pulses relative to the direct sync is determined by the DELAY No. 2 RANGE and 0.5-μSEC - 0.5 SEC controls. Initiation of the Delay No. 2 internal pulse is determined by the setting of the DELAY No. 2 FUNCTION switch. Now move the DELAY No. 2 FUNCTION switch to the AFTER DELAY No. 1 SYNC position, and note that the gate marking the delay interval is initiated after the No. 1 sync pulse.

So far the general operation of the Type 1392-A has been noted. The following is a more specific investigation of the instrument capabilities, circuit by circuit.

2.4 DETAILED OPERATION.

2.4.1 INPUT CIRCUITS. With all controls at their basic settings (paragraph 2.2) and a 2-volt-rms, 10-kc signal applied to the DRIVING SIGNAL terminal, connect the oscilloscope vertical input to the DRIVING SIGNAL terminal and the oscilloscope trigger input to the DIRECT SYNC OUT terminal. Set the oscilloscope sweep to view perhaps two cycles of the input signal. Remembering that the direct sync signal triggers the oscilloscope sweep, note the phasing effect of the TRIGGERING LEVEL control. Small disturbances in the input waveform result from the input triggering circuit transitions; the input selector switch selects either the positive-going or negative-going transition to trigger the direct sync. Set the input selector switch to NEG GOING AC and note the effect on the phase relation between the input signal and the direct sync.

At this point, it will be convenient to drive the Type 1392-A with a brief pulse rather than with a sine wave. If no such pulse is available from external equipment, the instrument can be caused to self-oscillate. Set the DELAY No. 1 controls for a 5-μsec delay, and the DELAY No. 2 controls for a 5-μsec delay. Set DELAY No. 2 FUNCTION switch to AFTER DELAY No. 1 SYNC. Feed the Delay No. 2 sync pulse to the DRIVING SIGNAL terminal. Adjust the TRIGGERING LEVEL control with the trigger selector switch set for POS GOING AC until the instrument indicator lamps glow steadily.

Now, with the oscilloscope sync output connected to the DRIVING SIGNAL terminal, observe the driving pulse, the direct sync pulse, and the Delay No. 1 gate pulse. Note that there is a delay between the driving pulse and the direct sync pulses. The nominal value of this delay is engraved between these terminals. Carefully adjust the COINC SENSITIVITY control and note the effect of the triggering level control on this delay. The small variations will be determined by the slope of the driving waveform and the exact point on this waveform where the instrument triggers.

If the exact time delay between a driving signal and one of the delayed sync pulses is to be known, this triggering delay must be established and added to the dial readings.

When the DELAY LINE FUNCTION switch is set in the DRIVING SIGNAL position, the input of the 0-1-μsec line is connected to the driving signal, and its output is from the DELAY LINE OUT

terminal. With the instrument operated from pulse drive as described above, set the DELAY LINE FUNCTION switch to the DRIVING SIGNAL position, and note the driving pulse at the DELAY LINE OUT terminal. Set the oscilloscope writing rate to 0.1 μsec/cm and vary the DELAY LINE setting from zero, noting that the input pulse is delayed. A comparison of the relative times of occurrence of this delayed driving signal and of the DIRECT SYNC signal will check the delay through the input circuits.

2.4.2 DELAY NO. 1. The first range of Delay No. 1 from 0-1 μsec is timed by the delay line. Set the DELAY LINE FUNCTION switch to 0-1 μsec, and observe this range. Connect the oscilloscope sync to the DIRECT SYNC OUT terminal and the oscilloscope vertical input to the No. 2 SYNC OUT terminal. Set the oscilloscope writing rate to around 0.2 μsec/cm and vary the DELAY LINE setting. The output from the delay line feeds the No. 1 sync circuits directly, and no gate is present at the No. 1 gate terminal.

Now set the DELAY LINE to 0.5 μsec, and set the 1-μSEC - 1 SEC dial and DELAY No. 1 RANGE switch to produce a 1-μsec delay. Set the oscilloscope writing rate for 1 μsec/cm. Observe the Delay No. 1 sync when the DELAY LINE FUNCTION switch is moved from the 0-1-μSEC RANGE position to the VERNIER position. Observe that the No. 1 gate is started after the 0.5-sec-delay-line-determined interval when the switch is in the VERNIER position.

The signal at the No. 1 GATE POS terminal produces this gate waveform at about a 5-volt level and at low impedance. A negative waveform at a 50-volt level and at 3000-ohm impedance level is available from the back panel of the instrument. With the DELAY LINE FUNCTION switch in the VERNIER position, set the controls for about a 5-μsec delay and observe this waveform on the oscilloscope.

Provision is also made to permit the Delay No. 1 circuits to be modulated by insertion of a signal on the back panel. To observe this action, set the DELAY No. 1 controls to 5 μsec and observe the gate on the oscilloscope when an ac signal (10-cycle to 100-kc) is fed into the TIME MODULATION jack (a standard two-wire microphone plug is required). For low frequencies, the maximum limit of modulating voltage will be found to be the maximum delay range. This is about 100 volts peak-to-peak or 35 volts rms when the 1-μSEC - 1-SEC dial is set at midscale. Connect the oscilloscope to the No. 1 SYNC OUT terminal and observe that this pulse is position modulated.

2.4.3 DELAY NO. 2, DELAY CIRCUIT FUNCTION. Return all controls to standard positions (paragraph 2.2). Connect the oscilloscope (1-μsec/cm writing rate) to the No. 2 POS GATE output terminal. Note that the No. 2 gate starts with the direct sync pulse. Move the oscilloscope vertical input to the No. 2 SYNC OUT terminal and note that the No. 2 sync occurs at the end of the gate interval. Now move the DELAY No. 2 0.5-μSEC - 0.5 SEC dial and observe its effect on the gate and sync pulse. Remember that a delay longer than the interval set by the generator will lead to irrational operation.

Now, while observing the No. 2 gate, note that the Delay No. 2 interval can be started after the Delay No. 1 interval if the DELAY No. 2 FUNCTION switch is set to the AFTER DELAY No. 1 SYNC position. Set the switch in this position and vary the DELAY No. 1 controls. Note the motion of the No. 2 gate.

2.4.4 COINCIDENCE OPERATION. Connect the oscilloscope to the Delay No. 2 POS GATE terminal, and set it to write at a 0.5 μsec/cm, 10-kc repetition rate. Set the instrument controls as described in paragraph 2.2, and then move the DELAY No. 2 FUNCTION switch to the COINC GATE position. Note that the No. 2 gate is started after the Delay 1 interval, and that the No. 2 sync pulse is formed on the leading edge of the No. 2 gate.

Now, reduce the COINC SENSITIVITY setting toward minimum until the No. 2 sync indicator lamp just extinguishes. The circuit is now armed for coincidence operation. The Delay No. 2 sync pulse will be formed only when a pulse is fed into the COINC PULSE DRIVE terminals and coincides with the gate "on" interval.

In order to observe and experiment with the coincidence system, coherent pulse trains must be available.

If a Tektronix Type 180 or equivalent time-marker generator is available, apply the 100-μsec pulse train to the DRIVING SIGNAL terminals and the 10-μsec pulse train to the COINC PULSE DRIVE terminals. (On the Tektronix 180 use the tip-jacks for the 10-μsec pulses to obtain maximum driving amplitude.) Set the COINC DRIVE switch to POS for train positive pulses at the COINC PULSE DRIVE terminals. Check that the other controls are set as described above. Now set the DELAY No. 1 controls to produce a delay of 55 μsec and the COINCIDENCE GATE controls for a duration of about 8 μsec. Observe the No. 2 positive gate on the oscilloscope set for a writing rate of about 10 μsec/cm. The picture should appear approximately as shown in Figure 1.3c. Note that the sixth 10-μsec pulse after the direct sync pulse appears superimposed in the center of the gate. Now move the oscilloscope input to the COINC PULSE OUTPUT terminal and note that an output corresponding exactly in time to the sixth 10-μsec pulse is present. Now, observing this output sync pulse, move the DELAY No. 1 controls about 5 μsec either way.

Note that when the gate starting time is moved beyond 60 or to less than 50 μsec the sync pulse is lost. Now repeat this experiment after increasing the COINCIDENCE GATE duration controls for a gate lasting 12 μsec. Note now that either one or two coincidence drive pulses will be selected. Longer gates will admit more pulses.

The foregoing illustrates the general principles and operation of the coincidence circuits. The limits of operation in frequency and input voltage may now be established if the coincidence driving pulse amplitude and frequency are varied. Reduce the coincidence gate duration to 0.5 μsec. Apply a 1-Mc pulse train to the COINC PULSE DRIVE terminals, and attempt to select individual 1-μsec pulses. If, after careful adjustment of the COINC SENSITIVITY control, it is not possible to select an individual 1-μsec pulse without the "leading edge" of the gate itself forming a sync pulse, then the amplitude of the 1-μsec driving pulses is inadequate (refer to Specifications). In this instance, or for that matter whenever the driving pulse amplitude is marginally low, the maximum possible coincidence sensitivity can be obtained by means of a short circuit placed on the No. 2 POS GATE terminals. Naturally, the usual monitor provided at these terminals will be lost, so amplification of the driving pulses is preferable if the equipment is available.

Since the coincidence gate can be reduced sufficiently in duration to permit selecting 1-μsec pulse periods, provision has been made to delay the No. 2 sync or coincidence pulse by means of the 0-1-μsec delay line interval. Set the DELAY LINE FUNCTION switch to DELAY No. 2 SYNC. Observe the Delay No. 2 sync pulse and then the pulse at the DELAY LINE OUT terminals as the DELAY LINE setting is varied from 0 to 1 μsec. In this function there is no electronic sync signal generator following the delay line, so some baseline ripples, pulse broadening, and amplitude decrease with increasing delay will be seen. These same effects will be found when a driving signal is passed through the line with the DELAY LINE FUNCTION switch in the DRIVING SIGNAL position.

Section 3

CIRCUIT DESCRIPTIONS

3.1 GENERAL. This section contains a sufficiently detailed description of the functioning of the individual circuits and components of the Type 1392-A Time-Delay Generator to enable the technician to service and calibrate the instrument with confidence. In general, the organization of this section will follow signal flow through the instrument, and reference will not be made to specific voltages, gains, etc. These data will be found in Section 5. Before reading or attempting to use this section, reread paragraph 1.5 for familiarization with the switching. The circuit diagrams fold out at the rear of this manual so that the individual circuits discussed in this and subsequent sections can be followed. For the sake of brevity, the action of the more common pulse circuits, Schmitt trigger, bistable, and blocking oscillator cannot be discussed in detail. Complete details about these circuits can be found in standard reference works.[1]

3.2 INPUT CIRCUITS.

3.2.1 GENERAL. Refer to the schematic diagram, Figure 5.5. The block diagram shows that this circuit system consists of three tubes which accept the input driving signal at J101, process it to form the direct sync pulse at J102, and provide a triggering signal for the other circuits in the instrument. These circuits permit control of the following input-signal characteristics by the operator:

a. He can select whether the input signal is a-c or d-c coupled to the trigger-generating circuits.

b. He can select whether a negative-going or positive-going slope of the input signal will cause the sync signal to be formed.

c. He can set, within a limited range, the d-c level at which the sync signal is formed. This operation is more complex than first appearances indicate, since by means of the TRIGGERING LEVEL control, the input sensitivity can be optimized for pulses of either polarity or for sine or square waves. When the latter waveforms have an amplitude greater than the minimum value, this control can be used to establish the direct sync pulse upon either zero-crossing of an input waveform.

3.2.2 AMPLIFIER, LIMITER AND SCHMITT TRIGGER CIRCUITS. Let us now follow a signal through these circuits. A signal applied at J101 is coupled either directly or via C101 to the grid of the input d-c amplifier, V101, through a limiter consisting

[1] E.g.: Millman and Taub, Pulse and Digital Circuits, McGraw-Hill, N.Y., 1956.

of silicon diodes D101 and D102. If there is a d-c component in the input signal, the input selector switch should be set on AC to prevent saturation of V101 and the limiter. The limiter is present to prevent shifts in the triggering level with higher input amplitudes. D-c coupling is provided expressly to permit triggering of the instrument on slowly varying signal voltages. The plate of the input amplifier (pin 1, V101) is directly connected to the input grid, (pin 2, V102) of a Schmitt trigger circuit.[2] The quiescent plate current of V101 sets the grid voltage of this circuit at a value near to that corresponding to the center of its hysteresis range. The exact value of this quiescent voltage is determined by R106, the TRIGGERING LEVEL control. For optimum sensitivity, R106 should be set to produce at pin 2 of V102 a grid voltage in the center of the hysteresis region. For positive pulses, the input is below the hysteresis region, and for negative pulses it is above the hysteresis region.

Assume now that a sinusoidal signal is applied at the DRIVING SIGNAL terminal. As the signal swings from negative to positive, the amplified signal at the plate of V101 swings the grid of V102 negative. V102 will switch so that the left-hand side goes off and the right-hand side comes on. If S101 is set for POS GOING drive, the positive transition of the left-hand side of V101 is coupled through contacts 101R and 112R to the grid (pin 2) of V101 via the differentiating circuit, C104 and R112. For negative-going drive, the opposite plate of the Schmitt circuit is selected by S101.

3.2.3 DIRECT TRIGGER GENERATOR AND BLOCKING OSCILLATOR CIRCUITS. The pulse-forming amplifier consisting of the pentode section of V101 is normally held in cutoff by fixed bias established by R112 and R113. It is turned on briefly when the Schmitt circuit switches. The pulse of plate current in this tube is drawn through winding 3-5 of T101, and induces a positive voltage at the grid (pin 3) of the blocking oscillator, V103.[3] This positive voltage removes a sufficient amount of bias to cause the oscillator to start. This bias is set by R128, R122, and R123. Note that the value of R128 may vary from one instrument to the next. It is chosen during calibration to produce a grid bias of -18.5 volts in the face of variation in the Thyrite units. The pulse of plate current in the blocking oscillator produces the negative direct trigger across R118 and the positive direct sync pulse coupled through the delay network L101, C107 to the grid (pin 8) of the output tube, V103. The positive direct sync pulse is produced across R124, and the negative pulse across R119. Sync output polarity is selected by S102.

3.2.4 DELAY LINE SWITCHING. The direct trigger is coupled to contact 101R of S301 to start the Delay No. 2 circuits in the AFTER DIRECT SYNC position of the DELAY No. 2 FUNCTION switch, and is also coupled to contact 103R of S202. S202 is the DELAY LINE FUNCTION switch, which determines whether the delay line triggers the Delay No. 1 sync-generating blocking oscillator in the 0-1-μSEC RANGE or simply delays the direct trigger by up to 1 μsec (the VERNIER position). Note that when the DELAY LINE FUNCTION switch is set in either DELAY LINE DIRECT position, the direct trigger is passed directly to V201 via contacts 103R and 105R to start the Delay No. 1 circuits. In this way, the Delay No. 1 circuit functions normally when the delay line is used for other purposes.

Inputs to the delay line in the two DELAY LINE DIRECT positions are through switch contact 112R of S202 for the DELAY No. 2 SYNC position, and contact 102R for the DRIVING SIGNAL position. Note that, in the DRIVING SIGNAL position, any d-c component in the input signal is blocked by C111. For the various positions of the DELAY LINE FUNCTION switch, S202, proper input and output terminating impedances are afforded by R215, R126, R131, and R132. These resistors are shown in Figure 5.5 with nominal values. They may be changed in instrument calibration to slightly different values to optimize performance with variations from one delay line to the next.

3.3 DELAY NO. 1 CIRCUITS. (See Figure 5.6.)

3.3.1 GENERAL. The action of the electronic circuits to produce the 1-μsec to 1-second Delay No. 1 sync is started by the direct trigger pulse from S202 applied via C204 to pin 2 of V202 to open the Delay No. 1 gate. When the gate is opened, the sweep generator, V203, is started. The slope of the sweep produced by this stage and by V204 is determined by R-C elements selected by the DELAY No. 1 RANGE switch, S201. When the sweep voltage rises to equal the reference voltage established by the 1-μSEC - 1-SEC control, the amplitude comparator (V205, V208, and V211) switches. The switching of the amplitude comparator produces a positive pulse, amplified in V206 and used to start the Delay No. 1 blocking oscillator, V207. The pulse of current in V207 sets the gate bistable to its off position, resets the sweep by turning V203 on, and ends the delay interval. Note that in the 0-1-μsec range, the delay line output is fed directly to V206 to start the blocking oscillator.

3.3.2 DELAY NO. 1 GATE. V201, the Delay No. 1 gate tube, is a bistable circuit.[4] The left-hand half of V201 is normally "on" and the high plate

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[2]Ibid, p. 164.

[3]Ibid, p. 282.

[4]Ibid, p. 140.

voltage (+150 volts) on the right-hand half keeps the grid (pin 2) of V203 positive with respect to ground and holds this tube in the "on" state. The cross-coupling network (R212 and R210) from the right-hand plate to the left-hand grid will permanently hold V201-left "on". Note that D202 and D203 are negative grid clamps that prevent the "off" grid of V201 from being more than 12 volts negative. The negative direct trigger pulse coupled through C204 and D201 will turn V201-left off and V201-right on. The resulting negative voltage at pin 2 of V203 will turn the sweep generator off and start a delay interval.

3.3.3 DELAY NO. 1 GATE AMPLIFIER. V202, the gate amplifier, is directly coupled to the left-hand plate of the gate through R205 and R206. When a delay interval is started, the rise in voltage at its grid causes its plate current to increase. A positive pulse is produced in R201 and a negative pulse at R202. The positive "gate" pulse is fed to J201 on the front panel and the negative pulse to J204 on the rear panel. Note that J204 is fed through C201, and hence is not capable of remaining flat over long-time intervals when a d-c load impedance is connected at J204.

3.3.4 DELAY NO. 1 SWEEP GENERATOR. V203 and V204 and their associated components comprise the circuit that produces the positive ramp establishing the Delay No. 1 interval. When the gate is triggered, pin 2 of V203 is driven negative with respect to ground. The slope of its rising plate voltage is set by the R-C network selected by S201, the DELAY No. 1 RANGE switch. The positive-going plate voltage of V203 is fed to pin 1 of V204, the bootstrap cathode follower. The rising cathode voltage at pin 3 of V204, coupled through C216, turns D205 off. The gain of this cathode follower is nearly unity, and the voltage at the top end of the sweep time-constant resistors is therefore nearly equal to that at the bottom ends. Thus, the current available to charge the sweep capacitors is nearly constant, and a linearly rising ramp is produced. The gain of the cathode follower, V204, is increased by a large cathode resistor, R236. When the delay interval is ended, this voltage must be rapidly returned to a low value. Fast reset is accomplished by the other half of V204, which is "off" during the active interval and is turned on by the gate coupled through R234 and C221 at the end of the active interval.

The reference time constant establishing the sweep slope is that of R225 and C212 (10-100-msec range). The slopes of all other ranges are adjusted to agree with this one during instrument calibration by means of the various range-calibrating potentiometers. In the 1-10-μsec range, some of the positive voltage from the gate bistable is inserted by C215 to establish the minimum delay accurately. C212 is used both on the 10-100-msec range and on the 100-msec-to-1-second range. In the 100-msec-to-1-second range the time constant is increased by a decade by increasing resistance (R226). A "step" must be inserted in this sweep to compensate for the reduced plate voltage on V203. This step is produced across R231, the 100-msec adjustment.

3.3.5 AMPLITUDE COMPARATOR. The rising sweep ramp is coupled to the grid (pin 7) of V208 in the amplitude comparator circuit. When the ramp rises to equal the voltage set by the 1-μsec-to-1-second control at pin 2, the circuit switches and resets the sweep. This equality is established by the amplitude comparator. Normally, with V203 conducting, the voltage at pin 7 will be less than that at pin 2, and the left-hand side will be "off". V205 can be compared to a bistable in which the normal grid-ground resistors of the cross-coupling networks are replaced by the plate resistance of V208. If the grid voltage at pin 7 is slowly increased so that it is just equal to that at pin 2, the circuit will still be stable with equal current in both halves of V208. Any increase in the voltage at pin 7 beyond this point will be amplified by this half of V208, and when the bias on V205-left has decreased sufficiently, V205 switches in a regenerative fashion with the left-hand half going "off" and the right-hand half turning "on". The positive pulse generated at the plate (pin 6) of the left-hand half of V205 produces the Delay No. 1 reset trigger.

The Delay No. 1 sweep voltage varies from about 10 to 110 volts with respect to ground over its control range. The voltages at the grids of V208 must follow this variation. V211 permits this voltage variation at the grids of V208 by establishing a constant current irrespective of voltage.

3.3.6 RESET TRIGGER GENERATOR, DELAY NO. 1 BLOCKING OSCILLATOR, AND INDICATOR CIRCUITS. The right-hand section of V206 is turned on by the positive pulse from the amplitude comparator and triggers the Delay No. 1 blocking oscillator. This circuit is identical in function and configuration to that of V102 and V103 in the input circuits (refer to paragraph 3.2). The pulse of plate current of V207-right develops a negative pulse across R244. This pulse is coupled through C209 and D204 to reset the gate bistable.

The positive Delay No. 1 sync pulse is used to turn V206-left off to light the indicator lamp V209. This positive pulse is coupled through capacitor C229, and causes the grid to draw current. This current charges C229, which discharges through R267, developing a negative voltage. This "grid-leak" bias voltage turns the tube off and causes its plate voltage to rise sufficiently to ionize V209. A single pulse will cause ionization and will register as a brief flash of light.

3.3.7 SWEEP REFERENCE VOLTAGE, SWEEP CLAMP, TIME-MODULATION INPUT CIRCUITS. The Delay No. 1 reference voltage corresponding to the setting of the 10-turn 1-μSEC - 1-SEC control, R262, is established by a voltage divider between 250 volts regulated and ground. R261 (Delay No. 1 minimum) and R263 (Delay No. 1 maximum) are used to set voltages corresponding to 10-msec and 100-msec delays respectively. The voltage established at the junction of R219 and R268 on the "ground" end of this voltage divider is applied to pin 6 of V203, the sweep clamp. When the sweep generator is conducting in the quiescent portion of the cycle, this diode conducts and stabilizes the quiescent value of the sweep voltages. Variations in plate resistance of the sweep generator tube from one tube to the next and with age are thereby minimized by both clamping action and feedback to the reference voltage divider.

Voltage from the time modulation jack (J203) is coupled in through C228 and developed across R260. Note that J203 is a short-circuiting jack. C228 is normally grounded to reduce noise at the grid (pin 2) of V208 and to minimize jitter. If it is desired to control Delay No. 1 with an external d-c signal, C228 can simply be shorted out and J208 permanently held open (or a plug-in C228 can be constructed to be used when no external signal is inserted).

3.3.8 AUTOMATIC RESET CIRCUIT. Since the delay gate is a bistable circuit, it must always receive a reset pulse to terminate the delay interval. Several conditions can arise that will disable this natural reset pulse momentarily. Once the amplitude comparator has fired and the gate bistable has failed to reset, the sweep will stay "up", and the circuit will be stable in this "locked-out" condition. An automatic resetting circuit (R259, C226, V210) provides a positive pulse at the grid of the gate bistable. This pulse will reset the circuit if the sweep is "up" for much more than a second. Under any normal circumstances the average voltage on C226 is too low to ionize V210, but on failure this voltage rises to 120 volts or more and V210 ionizes, resetting the gate.

3.4 DELAY NO. 2 AND COINCIDENCE CIRCUITS. (See Figure 5.7.)

3.4.1 GENERAL. The delay time interval is produced by circuits having configuration identical to those of Delay No. 1. The only differences are that the sweep generator and amplitude comparator are simplified and the triggering and output circuit configurations are different to accomodate the coincidence operation and to permit Delay No. 2 to be started after the Delay No. 1 interval.

In the block diagram, the three positions of the DELAY No. 2 FUNCTION switch are COINC GATE, AFTER DELAY No. 1 SYNC, and AFTER DIRECT SYNC, hereafter referred to as positions 1, 2, and 3, respectively. Note that the circuit connections to V303, the reset trigger generator, and to V306, the Delay No. 2 blocking oscillator, are the same in positions 2 and 3. In these two positions, only the input trigger pulse is changed, and the sync pulse is formed after the delay interval established by the sweep and amplitude comparator, as in the Delay No. 1 circuits. In positions 2 and 3, V303-right drives V306 to form the reset pulse for the gate and an output sync pulse.

In position 1, the COINC GATE setting of the switch, the Delay No. 2 gate is opened by the Delay No. 1 trigger pulse, but V303-right resets the gate directly to terminate the delay interval. The Delay No. 2 blocking oscillator is driven from the coincidence amplifier stage. In this stage the Delay No. 2 gate and the output of the coincidence pulse-amplifier stage are additively applied. Only a proper combination of these two signals will trigger the blocking oscillator to produce a sync pulse.

3.4.2 DELAY NO. 2 GATE. V301, the Delay No. 2 gate, is a bistable identical to that described in paragraph 3.3.2, in which the left-hand side is normally "on" and the right-hand side "off". The right-hand-side plate voltage is high (+150 volts) and the sweep generator (V302-left) is conducting at zero bias holding the sweep at a low, quiescent value of voltage. The negative trigger from either input circuits or Delay No. 1 circuits is applied through C301 and D301 to start the delay interval by turning V301-left off.

3.4.3 DELAY NO. 2 SWEEP CIRCUIT. When V302-left is in its quiescent state, it is "on" in zero bias, with a plate voltage less than 12 volts. V302-right acts as a clamp on this voltage by conducting when its cathode voltage is less than that across R315. This voltage is set by the current in the reference voltage divider made up of R330, R331, R332, R333, and R315. The clamping action stabilizes the quiescent conducting voltage and refers it to the reference voltage supplied to the amplitude comparator Schmitt circuit, V304. The time constant for each range is not individually adjusted; R317 is adjusted for the compromise in accuracy compared with the 500-msec-to-0.5-second-range time established by R319 and C307. Note that "steps" (R321 and R322) are provided in the two fastest sweeps for overcoming the effects of stray capacitance, and that C313 is provided to adjust the minimum end of the 0.5-μsec-to-5-μsec range.

3.4.4 AMPLITUDE COMPARATOR. V304, the Delay No. 2 amplitude comparator, is a Schmitt trigger circuit. The cathode voltage is set by the 0.5-

μSEC - 0.5-SEC control and the sweep is fed to the left-hand grid. Under quiescent conditions this grid will be negative with respect to cathode. When the sweep rises and nearly equals the cathode voltage, this side switches on and the right-hand side is rapidly switched off. The rising plate voltage at pin 6 of V304 forms a positive trigger voltage coupled through C315 to pin 7 of V303.

Note that the sweep generator is not linearized by "bootstrap" action, so that the sweep is exponential rather than linear. A linear dial calibration on the 0.5-μSEC - 0.5-SEC control is possible because V304 draws current from the tap on R332. The theoretical curve of voltage from this tap to ground is parabolic with angle. This parabola and the sweep exponential match very closely over the region of operation.

3.4.5 RESET, SYNC, AND INDICATOR CIRCUITS. When the DELAY No. 2 FUNCTION switch is set to COINC GATE, V303, the reset trigger generator, produces a negative pulse across R338. This pulse is coupled through C307 and D304 to reset the gate bistable. When used as a delay generator (i.e., in the other two positions of the DELAY No. 2 FUNCTION switch), the pulse of plate current passes through winding 3-5 of T301 and triggers the blocking oscillator. The blocking oscillator circuit is identical to circuits of the input and Delay No. 1 systems. When the blocking oscillator is triggered from the reset trigger generator, the negative reset pulse for the gate is formed in R355. The positive Delay No. 2 sync pulse drives the indicator amplifier (V307-left) to show the existence of the pulse. This circuit is identical to that described in paragraph 3.3.6.

The automatic reset circuit (R324, C302, and V309) is also similar to that described in paragraph 3.3.8.

3.4.6 COINCIDENCE AMPLIFIER AND COINCIDENCE INPUT CIRCUIT. When the switching is set for coincidence operation, the reset trigger generator closes the gate and terminates the delay interval. The coincidence sync pulse is produced by the blocking oscillator when it is triggered on by a pulse of plate current from V305, the coincidence amplifier. This pulse current will pass through winding 3-5 of T301 when the bias is removed from the grid (pin 1) of V305. V305 is biased by an adjustable d-c voltage derived in R342, the COINC SENSITIVITY control. The positive Delay No. 2 gate from pin 1 of V301 is added to this bias through R337, and can remove all or only a part of the bias. With the COINC SENSITIVITY control at MAX, all of the bias will be removed and the gate will cause V305 to draw current and to produce an output sync pulse on its "leading" edge. When the COINC SENSITIVITY control is moved toward MIN, V305 will not be switched on unless a coincidence driving pulse is added to the gate voltage through C320.

Note that J301, the No. 2 POS GATE terminal, is connected to the cathode of V305. Under normal circumstances, with the COINC SENSITIVITY control at MAX, the cathode current of V305 will produce the gate waveform as a positive pulse at this terminal. The amplitude of this pulse is adjustable by the COINC SENSITIVITY control. When coincidence driving pulses are added to the gate, they will be visible superimposed on the gate waveform at this point.

In order to produce a coincidence pulse, the drive to the coincidence amplifier must always be a positive pulse to add to the gate. If positive driving pulses are available, V307-left is used as a cathode follower and C320 is connected to the cathode by S303. When negative driving pulses are to be used, V307 is used as a phase inverter and C320 is connected to its plate.

V307, in addition to its use as a cathode follower or inverter, is also used as a compensator to balance the total current drain from the +250-volt regulated power supply. The network of R348, R365, and R363 sets its bias. This bias is controlled by the negative unregulated power supply. When the line voltage increases, there is a decrease in plate current in V307, which is set to compensate for the over-all increase in total drain from the +250-volt supply because of the higher heater voltages throughout the instrument. This compensation maintains exact heater voltage on the d-c heated tubes of Delay No. 1, and minimizes line drift of this delay.

3.5 POWER SUPPLY. (See Figure 5.8.)

3.5.1 GENERAL. A single power transformer supplies the two d-c supplies and the two a-c heater supplies. The two d-c supplies, of +365 and -265 volts nominal, are full-wave doublers using General Electric Type 1N1695 silicon rectifiers. The +365-volt supply feeds the electronic voltage regulator, VR401, which supplies +250 volts at 150 ma regulated. The 150-ma ground-return current of this regulated supply is passed through the heaters of V203 and V208, the sweep generator and amplitude comparator of the Delay No. 1 circuits. This regulated direct current decreases noise jitter and stabilizes these tubes against line transients. The drop across the two heaters in series has a nominal value of 24 volts, and across the heaters of V203, 12 volts. The 12-volt supply is used elsewhere in the instrument for bias.

The negative 265-volt unregulated supply feeds V401, which acts as a regulator to stabilize the -150-volt bias supply. This bias voltage is used

throughout the instrument for the d-c coupled gates, blocking oscillators, etc.

3.5.2 POSITIVE RECTIFIERS, FILTER CIRCUITS, AND 24-VOLT D-C HEATER POWER SUPPLY. Winding 9-10 of T401 produces a nominal 165 volts rms, which is supplied to the junction of RX401 through RX404. Two rectifiers are used in series to reduce back-voltage requirements. These rectifiers conduct on alternate half cycles of the a-c supply to charge C403 and C404. Approximately 390 volts is produced across these capacitors. The instrument current passes from the negative side of C404 through the heaters of V203 and V208 to ground. These heaters are paralleled with R406 and R407 to prevent open-circuiting of the supply if one of these tubes is accidentally removed or burned out. The heaters are bypassed by C405. The power-supply return current establishes the -24-volt supply voltage, and the drop across V203 and R407 establishes the -12-volt supply.

The +365-volt supply is applied to regulator VR401, which produces an accurately stabilized supply of +250 volts with very low hum and noise. (Less than 300 μf.) This voltage is stabilized to within 0.5 volt of +250 for a ±10% line-voltage change.

3.5.3 +250-VOLT REGULATOR. V501 and V502 are the series regulator tubes. V504 and the pentode section of V503 are the d-c amplifier tubes. V505, the reference tube, feeds a standard voltage to one grid (pin 7) of V504, while the regulated output voltage is fed from a voltage divider to the other grid (pin 2). The amplified difference voltage appearing at pin 6 of V503 is fed to pin 2 of V503. The triode section of V503 is used as a cathode follower to drive the series tube grids. Some unregulated dc is combined with the amplifier output at pin 2 of V503 to provide, through the voltage-divider network in the cathode (R512, R513, R514, R515, R517), a loop gain essentially infinite for input voltage changes.

C501 and R507 pass, in the correct phase, a sufficient amount of 120-cycle ripple to cancel the output ripple remaining after the regulator. Output voltage is set by the adjustment of R525 and the a-c gain of the regulator for ripple reduction is increased by C502.

In the event of an open circuit in either V208 or V203 by burnout or accidental removal of these tubes, the -24-volt bus will tend to become highly negative. If this occurs, V405 will ionize to cut off the left-hand side of V504 and turn the right-hand side fully on. This reduces the grid voltage of the series tubes to a minimum value and limits the current to a safe value, holding the -24-volt bus to less than -150 volts.

The d-c biasing potential for the positive heater bus is provided on the voltage regulator board by a voltage divider consisting of R510 and R523. This bus supplies V205 in addition to the series tubes and differential amplifier of VR401.

3.5.4 -150-VOLT BIAS CIRCUIT. Power transformer winding 11-12 provides a nominal a-c voltage of 103 volts rms, which is fed to the full-wave doubler consisting of rectifiers RX405 and RX406 and storage capacitors C407. A nominal output after the filter section (R404 and C407) is -265 volts with respect to ground. V401 serves as the regulator tube for the 12 ma of bias current. This tube is essentially a cathode follower. The gain with respect to line-voltage changes is increased by deriving the grid voltage for V401 from the +365-volt unregulated supply via R410 and R411, with R411 serving as the adjustment for the -150 volts. Neon tubes V402 through V404 drop approximately 180 volts as a reference voltage for the grid of V401. Ionization potential and sustaining current for these glow tubes are supplied by R413.

Section 4

CALIBRATION PROCEDURE

4.1 REQUIRED TEST EQUIPMENT. Beyond the usual requirements of accurate voltmeters required to establish the power-supply voltages, the essential equipment required for the calibration of a Type 1392-A Time-Delay Generator is an oscilloscope capable of being stably synchronized to the Type 1392-A and a source of accurately timed (preferably quartz-crystal-controlled) marker pulses. For the longer delay ranges a counter capable of time-interval measurements is a great convenience, but is not absolutely necessary. Two methods for calibration of the long delays are described in paragraph 4.4.1 and 4.5.1. If the oscilloscope to be used for calibration does not have a two-channel input circuit, then an R-C circuit capable of combining at least two channels of information should be constructed (see Figure 4.1). This adder must combine the synchronizing pulses and time-marker pulses used as references in calibration.

The following list of test equipment is preferred if the most efficient and accurate calibration is to be accomplished.

a. Time-mark generator (Tektronix Type 180A or equivalent)

b. Oscilloscope (Tektronix Type 541, 543, or 545, with Type 53/54-C plug-in front end, or equivalent)

c. Time-interval counter (General Radio Type 1130-A or equivalent)

d. Differential d-c voltmeter (John Fluke Type 801 or equivalent)

e. Distortion and Noise Meter (General Radio Type 1932-A or equivalent)

f. Delay line (General Radio Type 314-S86 0.5-μsec Variable Delay Line or equivalent)

g. Variac®, General Radio Type W5 or equivalent autotransformer.

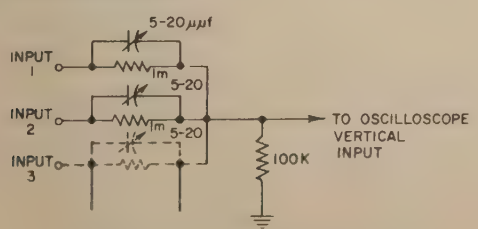


Figure 4.1. R-C Adder Network.

A complete recalibration of the instrument should never be necessary. The most common maintenance checks should be a measurement of the power-supply voltages and of the delay of the Delay No. 1 circuit on the 10-100-msec range at the 10- and 100-msec points. The most common source of error will be the range minimum drift due to aging of the sweep generator tubes, V203 and V302. Changes in dial calibration because of these tubes should be corrected by adjustment of the D1 MAX and MIN controls, R264 and R261, and the equivalent controls in the Delay No. 2 circuit. The Type 12AT7 sweep tubes, V203 and V302, should not be replaced unless the above-mentioned range minimum potentiometers are out of range or the tubes have burned-out heaters. These tubes are pre-aged and stabilized, and should be ordered for replacement by General Radio Type number 12AT7-1392. If they are replaced by "raw" tubes the dial calibration should be monitored frequently for the next 500 hours of use.

4.2 POWER SUPPLY ADJUSTMENTS AND CHECKS. To check for proper performance of the power supplies, first check that the line voltage is 115 volts. Then, with a d-c instrument known to be accurate to within ±0.5 volt, set B+ reg to +250 volts, and B- reg to -150 volts. Proper performance of the regulator is certain if: (1) line variation of 105 to 125 volts causes no more than a 1-volt change in the +250-volt supply, and (2) the same line variation causes no more than a 1-volt variation in the -150-volt supply.

A further performance check on the supply regulators is that the total noise from the two regulators, as measured on the General Radio Type 1932-A Distortion and Noise Meter, must be less than: (1) -74 db re 2 volts at 1 kc on +250 volts, and (2) -65 db re 2 volts at 1 kc on -150 volts as the line voltage is varied from 105 to 125 volts.

The only other power-supply adjustment is the line-voltage compensation, R363. This adjustment, described in paragraph 4.7.3, is set by measurement of the drift in Delay 1 with line variations.

4.3 INPUT CIRCUIT ADJUSTMENT. Only one check and one adjustment are required in the input circuits.

4.3.1 CHECK ON DELAY THROUGH INPUT SYSTEM.

a. Display the direct sync pulse on one oscilloscope channel.

b. Delay a brief pulse supplied to the prf drive terminals and passed through the 0-1 μsec delay line by connecting the other channel to the DELAY LINE OUT terminal. Set DELAY LINE FUNCTION switch to the DRIVING SIGNAL position. Rotate the DELAY LINE control until the two pulses match at the peaks (or at some other convenient reference point) and note the DELAY LINE reading. This is the delay through the input circuits.

4.3.2 DELAY LINE ZERO ADJUSTMENT. Set the DELAY LINE FUNCTION switch to the 0-1 msec range.

Set the DELAY LINE control to the zero mark. Combine the direct sync pulse and the Delay No. 1 sync pulse in the adder (Figure 4.1), or apply each to one channel of a dual-channel oscilloscope.

Now adjust C107 until the peaks of the two pulses coincide.

NOTE

Throughout the time measurements described in this section, times are always measured using the peaks of the 0.1-μsec sync pulses.

4.4 DELAY LINE CALIBRATION TEST (0-1-μSEC RANGE).

4.4.1 GENERAL. Set up the test equipment as shown in Figure 4.2. A time-mark generator capable of producing a 10-Mc (0.1-μsec) reference interval must be used. The trace linearity of any oscilloscope is inadequate and must not be relied upon.

4.4.2 CALIBRATION PROCEDURE.

a. Trigger the Type 1392-A at 10 kc from the marker generator.

b. Trigger the oscilloscope from the DIRECT SYNC OUT terminals.

c. Display DIRECT SYNC and DELAY No. 1 SYNC together. Set the DELAY LINE to check zero as in paragraph 4.3.2.

d. Now reference the 10-Mc train to DIRECT SYNC and DELAY No. 1 SYNC using the external delay line.

e. With the oscilloscope writing rate set at 0.1 μsec/cm or faster, move the DELAY LINE to 0.1 μsec, 0.2 μsec, 0.3 μsec, etc, and check registration with the 10-Mc train.

f. If a 10-Mc sine wave is used as the calibration reference, 0.15-, 0.25-, and 0.35-μsec points can be checked by simply recentering the oscilloscope trace to display the opposite peaks from those used in above.

g. Carry through check of cardinal points to 1.0 μsec as in e and f above.

h. If the DELAY LINE fails to meet its ±0.01-μsec specification the most probable reason will be aging of V206, and this tube should be replaced. A weakening of V206 will require more triggering voltage, and the actual delay produced will be longer than that read on the 0-1-μsec dial.

4.5 DELAY NO. 1 CALIBRATION.

4.5.1 GENERAL. The Delay No. 1 range is wide enough to require two methods of calibration. Method 1 is the same as that shown in Figure 4.2, in which the Delay No. 1 SYNC (or, for longer delays, the trailing edge of the gate) is registered with time markers from the time-mark generator. Method 2 requires the use of a counting time-interval meter started and stopped by the DIRECT and DELAY SYNC pulses. This second method is shown in Figure 4.3. Since this method has a resolution of 0.1 μsec even with the rapidly rising trigger pulses of the Type 1392-A and a 10-Mc counter, it can be used only for delays in excess of 100 μsec. The 1-to-10-μsec and 10-to-100-μsec ranges must be checked and calibrated by the first method. IN PERFORMING THESE CALIBRATIONS THE PRF

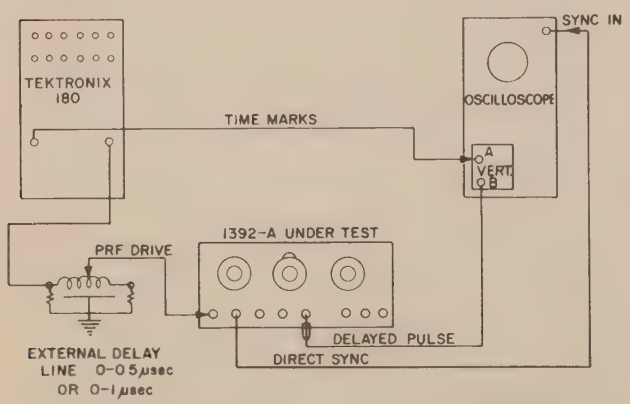


Figure 4.2. Equipment Setup for Time Calibration (Method 1).

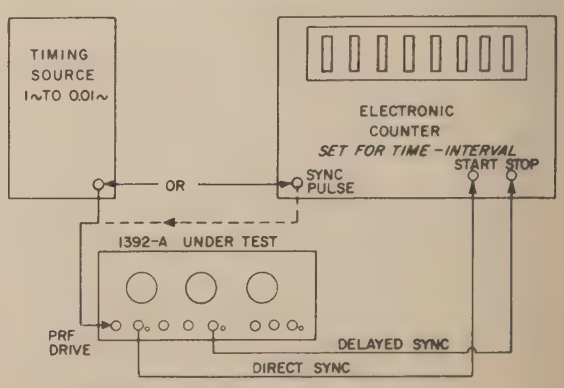


Figure 4.3. Equipment Setup for Counter Time Measurement.

DRIVE INTERVAL SHOULD ALWAYS BE AT LEAST 5 TIMES LONGER THAN THE MAXIMUM RANGE TO BE CALIBRATED.

4.5.2 CALIBRATION OF 10-100-MSEC RANGE.

a. Drive the instrument with 0.5-second or 1-second prf.

b. Use either Method 1 (displaying 10-millisecond markers) or Method 2.

c. Set 1-μSEC-1-SEC dial to 1.00. Set DELAY No. 1 RANGE switch to 10-to-100-msec position.

d. If Method 1 is used, calibrate the Delay No. 1 gate (sync pulse will be invisible). Make sure that start of oscilloscope display is in registration with a 10-millisecond marker.

e. Set D1 MIN (R261) for a 10-msec delay.

f. Move 1-μSEC - 1-SEC dial to 10.00, set D1 MAX (R263) for a 100-msec delay.

g. If very much adjustment of either potentiometer is necessary, repeat e and f until the two readings both check. There will be a small interaction.

4.5.3 CALIBRATION OF 100-MSEC TO 1-SECOND RANGE.

a. Set the prf to no more than 1 pulse per 5 seconds.

b. Set 1-μSEC - 1-SEC dial to 1.00, and set the DELAY No. 1 RANGE switch to the 100-msec to 1-second position.

c. Check the calibration at 100 msec against the counter (Method 2) or 100-msec marks.

d. If the delay is not 100 msec; set R231 (100 msec adjustment).

e. Set the 1-μSEC - 1-SEC dial to 10.00 and set R232 (1-second adjustment).

f. These two adjustments will interact; if much adjustment of either is necessary, the adjustments should be repeated until both are correct.

4.5.4 CALIBRATION OF DELAY NO. 1 RANGES BELOW 10 MSECS.

a. First make sure that the D1 MAX and MIN adjustments have been made on the 10-100-msec range. (Refer to paragraph 4.5.2.)

b. Using either the time-marker generator or the counter,

(1) set the 1-10-msec range at 10 msec by adjusting the 10-msec control (R230),

(2) set the 100-μsec-to-1-msec range at 1 msec by adjusting the 1-msec control (R229),

(3) set the 10-μsec-to-100-μsec range at 100 μsec by adjusting the 100-μsec control (R228).

c. Checks below 100 μsec will require the use of Method 1 (paragraph 4.5.1), since a 10-Mc counter does not have adequate accuracy. The calibration of the 1-10-μsec range below is an example.

(1) Set up equipment as shown in Figure 4.2.

(2) Set the instrument prf at 10 kc.

(3) Apply 1-μsec pulses from the marker generator.

(4) Register one of these marks with the DIRECT SYNC PULSE, using the external delay.

(5) Move the oscilloscope probe from DIRECT SYNC OUT to No. 1 SYNC OUT.

(6) With the 1-μSEC - 1-SEC dial at 1.00, and the DELAY No. 1 RANGE switch at 1-10-μsec, note the registration of the Delay No. 1 sync with the first 1-μsec mark after the reference mark.

(7) Adjust C315 (mounted underneath instrument on S201) for exact registration.

(8) Now move the 1-μSEC - 1-SEC dial to 10.00 and follow the 1-μsec timing comb to the tenth pulse. If the Delay No. 1 sync does not register, set the 10-μsec adjustment (R227).

(9) If either the 1- or 10-μsec adjustments are moved, return to the other end of the range and repeat the adjustment. The controls will interact slightly.

d. With the 1-kc prf and 10-μsec time markers, repeat step c for the 10-100-μsec range, checking the accuracy at the 10, 20, 30 ..... 100-μsec points. Adjust the 100-μsec adjustment with R228. If the 10-μsec point fails to track, R273 must be padded or replaced.

4.6 DELAY NO. 2 CALIBRATION.

4.6.1 GENERAL INSTRUCTIONS. The method of calibration of Delay No. 2 is exactly the same as that for Delay No. 1. Either time marks or, on the longer ranges, a counter can be used. Reread paragraphs 4.5.1, 4.5.2, and 4.5.3. Since Delay No. 1 is more accurate than Delay No. 2, Delay No. 2 can always be calibrated in terms of Delay No. 1 by direct comparison of sync pulses or gates.

4.6.2 50-MSEC TO 0.5-SECOND ADJUSTMENT.

a. Using Method 1, compare the Delay No. 2 gate with simultaneously displayed 100-msec pulses, or start and stop the counter with the direct sync and Delay No. 2 sync if the counting method is used.

b. With the DELAY No. 2 RANGE switch set at 50 msec to 0.5 second, and the 0.5-μSEC to 0.5-SEC dial set to 1, adjust D2 MIN (R333) for 50 msec.

c. Move the dial to 0.5 sec and adjust D2 MAX (R331) for registration with the fifth 100-msec pulse or for a counter reading of 0.5 second.

d. If either adjustment required appreciable resetting, repeat the adjustments until they converge.

4.6.3 0.5-μSEC TO 50-MSEC ADJUSTMENTS. For adjustments of 5, 50, 500 μsec, 5 msec, and 50-msec range maxima, R317 is set for a best compromise. Using either Method 1, Method 2, or comparison with the Delay No. 1 gate, set the 0.5-μSEC to 0.5-SEC dial to 5.00. Then set R317 to produce minimum deviation from the correct value for all

ranges (R-C components are ±1%, so the largest error will be less than ±2% after the compromise).

4.6.4 DELAY NO. 2 1.0-μSEC ADJUSTMENT.

a. Use either Method 1 or set the DELAY LINE FUNCTION switch to the 0-1-μsec range and the DELAY No. 2 FUNCTION switch to AFTER DIRECT SYNC.

b. Compare a 1-μsec Delay No. 1 sync pulse with a Delay No. 2 sync pulse and set C312 for registration of these pulses.

4.7 JITTER AND LINE-DRIFT CHECKS AND ADJUSTMENTS.

4.7.1 GENERAL. The setup for jitter measurements is shown in Figure 4.4. It is necessary to establish a source of lower-frequency driving pulses essentially jitter-free relative to the higher-frequency pulses used as a reference. The pulse dividers of most time-mark generators are satisfactory sources. Since the switching rates are fast, very little jitter is produced.

4.7.2 JITTER MEASUREMENT AT 1 AND 10 MSEC, DELAY NO. 1 CIRCUIT.

a. Set up equipment as shown in Figure 4.4.

b. Display 1-μsec timing comb on the oscilloscope (set to write at about 1 μsec/cm).

c. Synchronize the Type 1392-A at a 100-cycle rate (10 msec).

d. Set the DELAY No. 1 controls for 1-10-μsec range, 1-μsec delay.

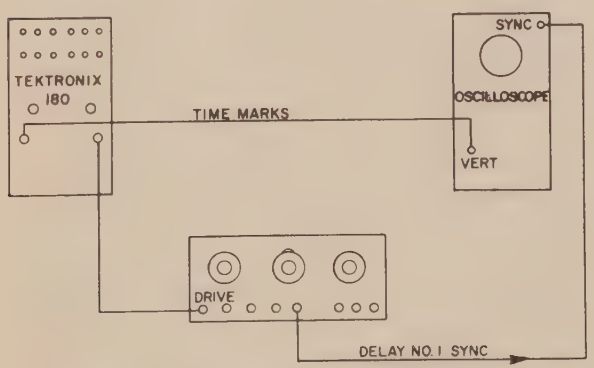


Figure 4.4. Apparatus for Jitter Measurements.

e. Synchronize the oscilloscope with the Delay No. 1 sync pulse.

f. Note that the 1-μsec pulses displayed on the oscilloscope show no visible jitter. (If jitter is present at this point, adjust sync drive controls on both the Type 1392-A and oscilloscope. If jitter is still present, check 10-msec comb and 1-μsec comb from time-mark generator for stability.)

g. Now set DELAY No. 1 controls for 1-msec delay.

h. Note that just after switching ranges the sync pulse will drift for about a minute. Allow this drift to stop. Note any jitter of 1-μsec pulse comb. There should be less than 0.02 μsec of fluctuation in pulse position. (The oscilloscope writing rate can be expanded to 0.1 μsec/cm and the Delay No. 1 control moved to display a single 1-μsec pulse at this point.)

i. Now drop the prf to that for a 100-msec (or 50-msec) period, and check jitter at 10 msec on the 1-10-msec range, and at 10 msec on the 10-100-msec range.

NOTE

There will be about 5 or 10 times the jitter at 10 msec on the 10-100-msec range as at the 10-msec point on the 1-10-msec range. The signal-to-noise ratio is less at the bottom end of a range; in fact, the noise on each range is about constant.

j. If the jitter of Delay No. 1 is appreciably greater than 1:50,000 at the minimum "end" of either range measured above, measure the power-supply noise (refer to paragraph 4.2). If the power-supply noise is not excessive, readjust the ground loop over the power transformer for minimum jitter.

4.7.3 LINE-DRIFT ADJUSTMENT.

a. Set up the instruments exactly as for the jitter measurement described in paragraph 4.7.2.

b. Check jitter at 1 msec.

c. Now, observing the 1-μsec timing pulses at a 1-msec delay, vary the line voltage applied to the instrument from 105 to 125 volts. (Use a Variac® and an a-c voltmeter.)

d. Observe any slow drift that occurs in the position of the 1-μsec timing pulses. If the drift is in excess of 0.1 μsec, reset R363, the LINE BAL control on the rear shelf, to minimize this drift.

Section 5

SERVICE AND MAINTENANCE

5.1 GENERAL. The two-year warranty given with every General Radio instrument attests the quality of materials and workmanship in our products. When difficulties do occur, our service engineers will assist in any way possible.

In case of difficulties that cannot be eliminated by the use of these service instructions, please write or phone our Service Department, giving full information of the trouble and of steps taken to remedy it. Be sure to mention the serial and type numbers of the instrument.

Before returning an instrument to General Radio for service, please write to our Service Department or nearest district office (see back cover), requesting a Returned Material Tag. Use of this tag will ensure proper handling and identification. For instruments not covered by the warranty, a purchase order should be forwarded to avoid unnecessary delay.

5.2 SERVICE PROCEDURE. The Type 1392-A Time-Delay Generator is designed for easy servicing. There are many front-panel connections to the circuits and many switching combinations to isolate various circuit groups. Wherever a stage does not have a front-panel connection, labeled test points are available. The following service notes are therefore based on signal-tracing techniques.

First, isolate the trouble by careful observation of the front-panel indications, establishing the presence or absence of signals or any defect in signal characteristics. When it has been definitely established that a trouble exists (read paragraph 5.3 carefully), remove the instrument cover and obtain the additional data necessary by observing voltages, neon indicator lamps, and test-point waveforms. These observations, coupled with the data in paragraph 5.4, should permit any trouble to be quickly isolated.

CAUTION

Do not pull out and replace tubes when the instrument power is on. Removal of V203 or V208 from their sockets subjects many components to a higher voltage than necessary.

Take extreme care when measuring voltages on the etched board. An accidental heater short circuit may permanently damage the etched wiring pattern.

When replacing a component on an etched board, be careful not to destroy the bond between board and etched wiring by heat or by force. When removing the defective component, firmly grab the wire at the component side (the component may be clipped off first), and then, pulling on the wire, apply just enough heat to the solder to free it. Before inserting the new component, make certain that an unobstructed passage exists, either by carefully drilling through the component side or by removing the solder from the hole. When using the soldering iron to remove solder, draw the solder back along the conductor from the tab with quick strokes. Never apply the soldering iron to the etched board for more than five seconds at a time.

If the position of the board prohibits the above procedure, many components can be replaced as follows: destroy the old component, preserving enough wire to attach the replacement, then solder the new component in place.

5.3 TROUBLE-SHOOTING PROCEDURE.

5.3.1 GENERAL. Field experience with the Type 1392-A and with other instruments of its type shows that certain operational errors and common system difficulties give the indication of trouble when none really exists within the instrument itself. If the instrument does not appear to be working correctly, read this section first and carefully check the Type 1392-A and the system in which it is used to be sure that controls are correctly adjusted, all fittings and grounds are tight, and that the Type 1392-A is not triggering on noise.

5.3.2 ERRATIC SYNC OR GATE PULSE GENERATION NOT NECESSARILY SYNCHRONIZED TO DRIVING SIGNAL, SPURIOUS SIGNALS, ETC.

5.3.2.1 Delay Too Long for PRF. The most common cause of this difficulty is an error in setting the delay controls, so that a delay interval longer than the time base is set. The Type 1392-A will be stable to considerably more than one-half of the interval set by the prf drive. Calculate the time interval represented by the prf driving signal and carefully check the Type 1392-A switch and dial settings. Observe maximum duty-ration specifications.

5.3.2.2 Noise or Harmonics in Driving Signal. The Type 1392-A input circuits are very sensitive. Check ground between instrument and driving source. Check driving source for hum, spikes or noise related to the production of the driving signal (ringing, etc). Remember that any noise over 0.1 volt might trigger the Type 1932-A.

a. Refine input TRIGGERING LEVEL control.

b. Attenuate input signal.

c. "Clean up" input signal (by terminating coax, for example).

5.3.3 DELAY NO. 2 GATE MISSING, SYNC PULSE NORMAL. The COINC SENSITIVITY controls the amplitude of this signal in all positions of the DELAY No. 2 FUNCTION switch. Turn the control in a clockwise direction.

5.3.4 INPUT CIRCUITS LACK SENSITIVITY, APPARENT LOW INPUT IMPEDANCE AT HIGHER PRF DRIVE FREQUENCIES. The DELAY LINE FUNCTION switch is set in a DELAY LINE DIRECT position, and loads input circuit. Set switch to VERNIER position.

5.3.5 EXCESSIVE RINGING ON A SYNC PULSE.

a. Incorrect cable termination. All sync output systems are 94 ohms. Cables should be of correct impedance, and long cables should be terminated in correct impedance to prevent difficulty at receiving end.

b. Avoid open-wire leads for best sync pulse shape.

c. Some ringing on Delay No. 2 sync will be observed when the DELAY LINE FUNCTION switch is set to the DELAY No. 2 SYNC position. This is normal, since the line is not perfectly matched. If the line is not needed in this position, set the switch to the VERNIER position.

5.3.6 OVERSHOOT ON GATE WAVEFORMS. The gate waveforms are not carefully controlled in shape at all durations. They are simply intended as oscilloscope markers to aid in identifying the delay interval. Some overshoot, ramp-off, and variation of amplitude with duty-ratio is normal.

5.3.7 NO SYNC PULSE OUTPUT, MONITOR LAMP OUT. Place sync pulse polarity switch in the negative position. If the lamp comes on, the trouble is probably a shorted cable. Check Type 874 Coaxial panel fitting for damage, such as broken tine in the inner conductor.

5.4 SYSTEMATIC TROUBLE SHOOTING.

5.4.1 GENERAL. This section is based entirely upon symptoms observed at the front panel of the instrument. The service technician is urged to study carefully the symptoms before removing the instrument from its box. A great deal of time can be saved by having all the "clues" on hand before starting on the search for the trouble.

Unless there is an obvious defect, such as a smoking component, set the instrument controls to the standard positions noted below and determine whether the front panel fittings are producing their proper signals and the indicator lamps are giving their proper indications. Once the defective circuit group is isolated and the cover is removed, it is a good idea to examine carefully:

a. the tubes of the defective group. See that they are lighted and that their electrodes are of normal color. (Some tubes may glow a bit blue because of gas.)

b. condition of components. This instrument has well-derated resistors. There should be no discoloration of paint or of color codes.

c. those components specifically mentioned as pertinent to the circuit group suspected from the front panel conditions described in the balance of this section.

Standard input conditions and switch settings:
PRF drive: Over 1 volt, 10 kc, free from noise and transients.
Triggering switch: POS GOING AC
TRIGGERING LEVEL: CENTERED
DELAY LINE FUNCTION: VERNIER
DELAY No. 1 RANGE: 1-10 μsec
DELAY No. 1 1 μSEC - 1 SEC: 1.00
DELAY No. 2 FUNCTION: AFTER DIRECT SYNC
COINC SENSITIVITY: Fully clockwise
DELAY No. 2 RANGE: 5-50 μsec
DELAY No. 2 .5 μSEC - 0.5 SEC: 1.0

Observe:

1. Direct sync pulse
2. No. 1 gate
3. No. 1 sync
4. No. 1 sync indicator
5. No. 2 gate
6. No. 2 sync
7. No. 2 sync indicator

5.4.2 DRIVE PRESENT; ALL OTHER SIGNALS ABSENT. First check the input signal, then try adjusting the TRIGGERING LEVEL control. If this is of no help, the trouble is either in the input trigger circuit group or in the power supply. Check that there is +250 volts at the blue lead on VR402 etched board, and -150 volts at the green lead at pins 2 and 7 of V402.

If V405, the neon lamp at the corner of power-supply etched board, is glowing brightly, turn the instrument off. Check V203 and V208 for open heaters, and check the -20-volt wiring.

If all voltages are correct, check V101, V102, V103, and check waveforms at test points TP101-104.

5.4.3 DRIVE PRESENT. RANDOM OUTPUT PULSES FROM ALL TERMINALS. INDICATOR LAMPS GLOWING. Check the -150-volt bias-supply voltage.

5.4.4 ONLY DIRECT SYNC PULSE ABSENT. OTHER CIRCUITS OPERATE NORMALLY. J102 shorted or V103 defective. Check circuits around V103.

5.4.5 DIRECT SYNC, DELAY NO. 2 SYNC PRESENT; DELAY NO. 1 GATE AND SYNC ABSENT. Defect is on Delay No. 1 circuits. Throw the DELAY LINE FUNCTION switch to the 0-1-μsec position. If the sync is still absent, refer to paragraph 5.4.5.1. If the sync is present, refer to paragraph 5.4.5.2.

5.4.5.1 No. 1 Sync Absent with DELAY LINE FUNCTION Switch in Either VERNIER or 0-1-μsec Position.

a. Set the DELAY LINE FUNCTION switch to the DELAY No. 2 SYNC position. If the Delay No. 1 monitor light comes on, then the defect must be in the delay line itself or in its wiring or switching.

b. If the No. 1 sync pulse is still absent, then the defective tube or component must be associated with V206 or V207. Check waveforms at TP204, TP205, and check voltages and components associated with these stages.

5.4.5.2 No. 1 Sync Absent With DELAY LINE FUNCTION Switch in VERNIER Position, Present With Switch in 0-1-μsec Position. Placing the DELAY LINE FUNCTION switch in 0-1-μsec position and establishing the fact that the instrument operates eliminates V206 and V207. The difficulty must lie in the gate, sweep generator, or amplitude comparator. Proceed as follows:

a. Remove the cover of the instrument.

b. Observe the Delay No. 1 automatic reset lamp (V210) with the prf drive (10 kc) applied. If the bulb flashes intermittently, proceed to (1) below. If not, refer to (2).

(1) Delay No. 1 automatic reset bulb flashing: This indicates that the sweep voltage is high. The sweep generator tube, V203, is off, the right-hand tube of the gate is on, and the amplitude comparator is set into "active state" and will be stable in this position. The trouble may be the amplitude comparator V205, V202, V211, the sweep generator V203, or the bistable gate V201. The possibility that V206 is weak should not be overlooked, since the signal at its cathode in the 0-1-μsec range is larger than its grid drive. Test point waveforms are of little use in locating this trouble. A systematic replacement of tubes with tubes known to be functioning (exchange with Delay No. 2) and then a check of voltages against Table 5 is the best procedure.

(2) Delay No. 1 automatic reset lamp not flashing. This indicates that the sweep voltage is never rising. Beyond some possibility of a grid-cathode short in V208, the amplitude comparator is eliminated. Most likely source of trouble is V201. Check V201 by substitution. Check D201 and D203. Check V203 (turn instrument OFF before unplugging V203). Check D205 for an open circuit. If these actions do not help, check the d-c voltages on V201 and V203 against Table 5.

5.4.6 DIRECT SYNC, DELAY NO. 1 SYNC, AND DELAY NO. 2 SYNC AND GATE PRESENT. DELAY NO. 1 GATE ABSENT. Only the gate amplifier tube, V202, is involved. Check this tube. If it is all right, check its associated components.

5.4.7 DIRECT SYNC, NO. 1 GATE AND SYNC, NO. 2 SYNC ALL PRESENT. NO. 2 GATE MISSING. If the COINC SENSITIVITY control is fully clockwise and the panel fitting is not damaged and short-circuiting, then V305 or one of its associated components is defective. Check the tube and its components.

5.4.8 DIRECT SYNC, NO. 1 GATE AND SYNC, NO. 2 GATE PRESENT. NO. 2 SYNC MISSING. The only tube not directly involved in the delay and resetting circuit for the No. 2 delay is the sync blocking oscillator. Check V306 and its components. Make sure that the coaxial connector has not been damaged.

5.4.9 DIRECT SYNC, DELAY NO. 1 SYNC, AND GATE ALL PRESENT. DELAY NO. 2 SYNC AND GATE ABSENT. This set of symptoms indicates a failure somewhere in the delay loop. There are two types of failure immediately recognizable. Remove instrument cover. If the Delay No. 2 automatic reset lamp is flashing, refer to (1) below. If it is not flashing, refer to (2).

(1) Delay No. 2 Automatic Reset Lamp Flashing. This indicates that V302, the sweep generator tube, is off and the sweep voltage is high. The amplitude comparator has not reset the gate. The gate itself is probably all right. If the reset bulb stops flashing when the prf drive is removed, the gate and V302 almost certainly are all right and need not be tested. First check V302, V304, and V303 by replacement with tubes known to be good and then check their electrode voltages. If light continues to flash even when there is no drive, check V301 and V302.

(2) Delay No. 2 Automatic Reset Lamp, V309, Not Flashing. These symptoms show that the sweep voltage at the grid of V304 never rises. Either the gate never opens V302, or the triode section of V303 is defective. First check these tubes. If they are all right, check the diodes in gate circuits. Then check the gate d-c voltages (Table 5).

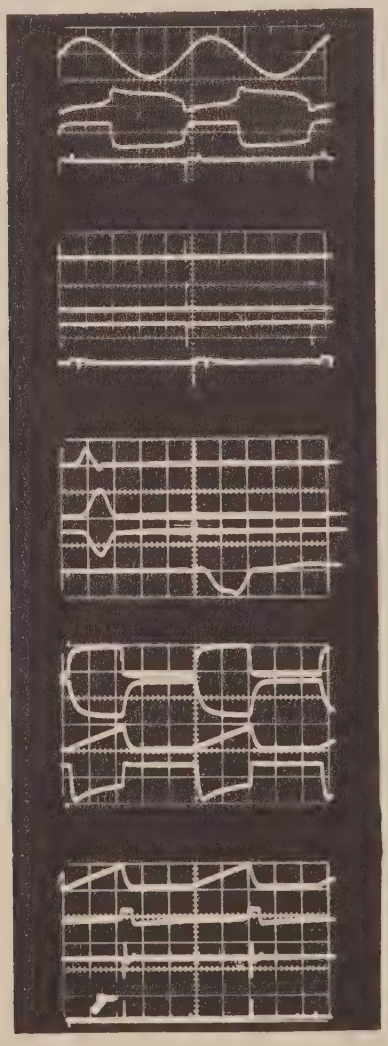
5.4.10 ALL OUTPUTS NORMAL, NO COINCIDENCE PULSES APPEAR ON COINCIDENCE GATE, PULSE INPUT PRESENT AT COINCIDENCE DRIVE TERMINALS. The only stage involved is V307. Check this tube and its associated components.

5.4.11 EITHER SYNC MONITOR LAMP GLOWS CONTINUOUSLY, WHETHER OR NOT SYNC IS PRESENT. The only possibility is the monitor amplifier. Check and, if necessary, replace V307 and V206.

5.4.12 EITHER SYNC MONITOR LAMP FAILS TO LIGHT WHEN SYNC IS PRESENT. Again, difficulty is probably associated with amplifier tube, V307, or with V206. If a new tube fails to remedy the difficulty, check components from the input coupling capacitor of these stages onward.

5.5 TROUBLE-SHOOTING IN POWER SUPPLIES.

5.5.1 GENERAL. Power-supply trouble-shooting is straightforward. It is complicated only slightly by the presence of the vacuum-tube regulator circuits. These regulators will hold their output voltage for a time as rectifiers or filters deteriorate, but then will fail first at low line input when all of their reliability margins are used up. If the output of a power supply is low, first check the unregulated input voltage (115-volt line) against the nominal value listed on page 24. If the input voltage is normal, then the regulator circuit can be checked by tube replacement or voltage measurements. Higher-than-normal output voltage probably indicates a defective series-regulator tube or a defective amplifier tube in VR401. Excessive hum or noise on the +250-volt regulated bus probably indicates a defective amplifier tube in VR401, and these tubes should be checked. The most critical tube in this respect is probably V503.



1. PRF 100 KC, WRITING RATE 2μSEC/CM.
   - A. INPUT SIGNAL, 5V/CM
   - B. TP101 50V/CM
   - C. TP102 50V/CM
   - D. TP103 50V/CM

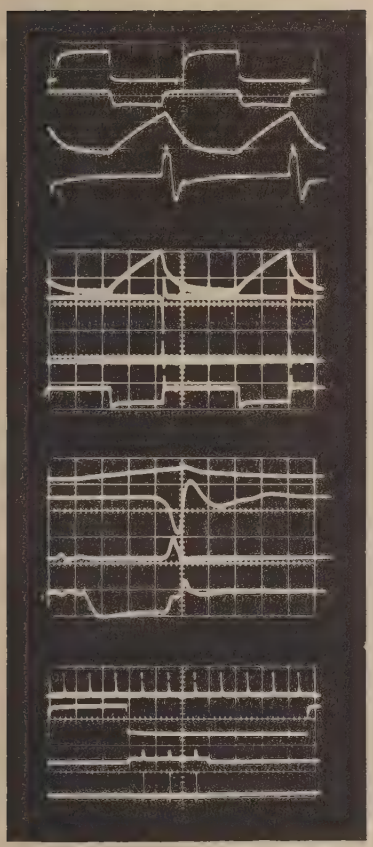
2. PRF 100 KC, WRITING RATE 2μSEC/CM, 0.5-μSEC DELAY.
   - A. TP104 20V/CM
   - B. POS DIRECT SYNC 20V/CM
   - C. NEG DIRECT SYNC 20V/CM
   - D. PIN 7 V206 (S202, 109R) 10V/CM

3. PRF 100 KC, WRITING RATE 0.1 μSEC/CM, 0.5-μSEC DELAY.
   - A. TP104 20V/CM
   - B. POS DIRECT SYNC 20V/CM
   - C. NEG DIRECT SYNC 20V/CM
   - D. PIN 7 V206 (S202, 109R) 10V/CM

4.
   - A. POS DELAY NO. 1 GATE 5V/CM
   - B. NEG DELAY NO. 1 GATE (4 μSEC DELAY) 5V/CM
   - C. TP202 50V/CM
   - D. TP201 20V/CM

5.
   - A. TP202 50V/CM
   - B. TP203 20V/CM
   - C. TP204 200V/CM
   - D. TP205 10V/CM

Figure 5.1. Test Waveforms for Trouble-Shooting.



6. DELAY NO. 1, 4 μSEC; DELAY NO. 2, 4 μSEC.
   A. POS GATE, DELAY NO. 2 5V/CM
   B. TP301 20V/CM
   C. TP302 50V/CM
   D. TP303 5V/CM

7. DELAY NO. 1, 4 μSEC; DELAY NO. 2, 4 μSEC.
   A. TP302 50V/CM
   B. TP304 10V/CM
   C. TP306 10V/CM
   D. TP305 5V/CM

8. DELAY NO. 1, 0.1 μSEC; DELAY NO. 2, 0.7 μSEC. 0.2 μSEC/CM.
   A. TP302 50V/CM
   B. TP304 100V/CM
   C. TP306 100V/CM
   D. TP305 10V/CM

9. PRF 10 KC, DELAY NO. 1 35 μSEC, DELAY NO. 2 30 μSEC.
   (Set DELAY LINE FUNCTION switch to VERNIER and DELAY NO. 2 FUNCTION switch to COINC DRIVE.)
   A. 10-μSEC PULSES FROM 180-A TO POS COINC, 10V/CM
   B. 30-μSEC DELAY NO. 1 GATE, 5V/CM
   C. 30-μSEC DELAY NO. 2 GATE, 5V/CM
   D. TP305 100V/CM

Figure 5.1. Test Waveforms for Trouble-Shooting. (Continued)

TABLE OF VOLTAGES AND RESISTANCES

TUBE (TYPE)	PIN	DC VOLTS		RES TO GND
		TRIG LEVEL CCW	TRIG LEVEL CW	
V101 (6U8)	1	+106	+40	51 k
	2	-5.9	-5.8	10 k
	3	+228	+228	18 k
	6	+245	+245	1.1 k
	8	+2.7	0	1 k
	9	0	-0.2	2 k
V102 (6BQ7)	1	+190	+245	3.9 k
	2	+106	+40.5	54.5 k
	3	+106	+77	6.8 k
	6	+250	+197	5.1 k
	7	+58	+75	56 k
	8	+106	+77	6.8 k
V103 (6350)	1	+245	+245	1.5 k
	2	-21	-21	30
	3	-39	-39	35 k
	6	+245	+245	1.1 k
	7	-21	-21	130
	8	-39	-39	35 k
V201 (5965)	1	+104		8 k
	2	-0.45		2.5 k
	3	0		0
	6	+140		8 k
	7	-12.3		2.5 k
	8	0		0
V202 (6AU6)	1	-12		85 k
	2	0		390
	5	+250		6.8 k
	6	+150		10.8 k
	7	0		390
V203 (12AT7)	1	+17		540 k
	2	0		60 k
	3	0		0
	4	0		0
	5	-12		11
	6	+17.5		1.8 k
	7	+17.5		1.8 k
	8	+17		540 k
V204 (5965)	1	+250		0
	2	+17.3		510 k
	3	+22.5		10 k
	6	+22.5		10 k
	7	-0.7		2.7 M
	8	0		100
V205 (5965)	1	+250		3 k
	2	+195		32 k
	3	+205		37.5 k
	6	+235		3 k
	7	+205		143 k
	8	+205		37.5 k

TUBE (TYPE)	PIN	DC VOLTS	RES TO GND
V206 (6U8)	1	+17.5	240 k
	2	-6	34 k
	3	+13.5	30.5 k
	6	+250	1.1 k
	7	+13.5	
	8	-21.8	22
	9	-21	18 M
V207 (6350)	1	+250	1.1 k
	2	-24	130
	3	-43.5	135 k
	6	+250	1.18 k
	7	-24	32
	8	-43.5	135 k
V208 (5751)	1	+195	32 k
	2	+27	515 k
	3	+29	
	4	-24	11
	5	-12	11
	6	+205	143 k
	7	+17	540 k
	8	+30	
V211 (5751)	1	+30	
	2	-75	500 k
	3	-74	150 k
V301 (5965)	1	+103	8 k
	2	-0.4	2.5 k
	3	0	0
	6	+140	8 k
	7	-12.3	2.5 k
	8	0	0
V302 (12AT7)	1	+19.2	210 k
	2	0	60 k
	3	0	0
	6	+12	1.2 k
	7	+12	1.2 k
	8	+19.3	210 k
V303 (6AU8)	1	+26	15 k
	2	+19	215 k
	3	+250	0
	6	+6	1 k
	7	0	33 k
	8	+160	82 k
	9	242	5 k
V304 (12AX7)	1	+223	47 k
	2	+26	15 k
	3	+39	9 k
	6	+240	5.6 k
	7	+38	28 k
	8	+39	9 k

TABLE OF VOLTAGES AND RESISTANCES

TUBE (TYPE)	PIN	DC VOLTS	RES TO GND
V305 (6485)	1	-76	80 k
	2	0	240
	5	+250	390
	6	+250	47 k
	7	0	240
V306 (6350)	1	245	1.15 k
	2	-23.3	30
	3	-40	38 k
	6	+250	1.1 k
	7	-23	120
	8	-40	38 k
V307 (5965)	1	+230	5.6 k
	2	+8.6	235 k
	3	+12.5	5.6 k
	6	+30	235 k
	7	-22.3	18 M
	8	-21.5	20
V401 (6AU6)	1	-156	430 k
	2	-155	15 k
	5	0	0
	6	0	0
	7	-155	15 k
V501 (6AV5GA)	1	240	490 k
	3	260	82
	5	400	85 k
	8	395	86 k
V502 (6AV5GA)	1	240	490 k
	3	260	82
	5	400	85 k
	8	395	86 k
V503 (6AN8)	1	400	85 k
	2	232	2.7 M
	3	242	470 k
	6	232	2.7 M
	7	250	0
	8	150	72 k
	9	153	47 k
V504 (5965)	1	153	47 k
	2	38	500 k
	3	40.5	5.5 k
	6	250	30 k
	7	36.6	50 k
	8	40.5	5.5 k
V505 (5651)	1	84	46 k
	5	84	46 k
	7	0	0

NOTES

1. Set panel controls as follows:

TRIGGERING LEVEL:	Counterclockwise (unless otherwise noted)
Trigger selector:	POS GOING AC
DELAY LINE:	0
1 μSEC - 1 SEC:	0
DELAY LINE FUNCTION:	0-1 μSEC RANGE
DELAY NO. 1 RANGE:	10 - 100 ms
COINC SENSITIVITY:	Counterclockwise
DELAY NO. 2 FUNCTION:	AFTER DIRECT SYNC
COINC DRIVE:	POS
DELAY NO. 2 RANGE:	5-50 ms
DIRECT SYNC OUT:	+
NO. 1 SYNC OUT:	+
NO. 2 SYNC OUT:	+

2. Measure resistance with B+ grounded.

3. Measure voltages with no input signal.

4. Resistances are in ohms unless otherwise indicated.

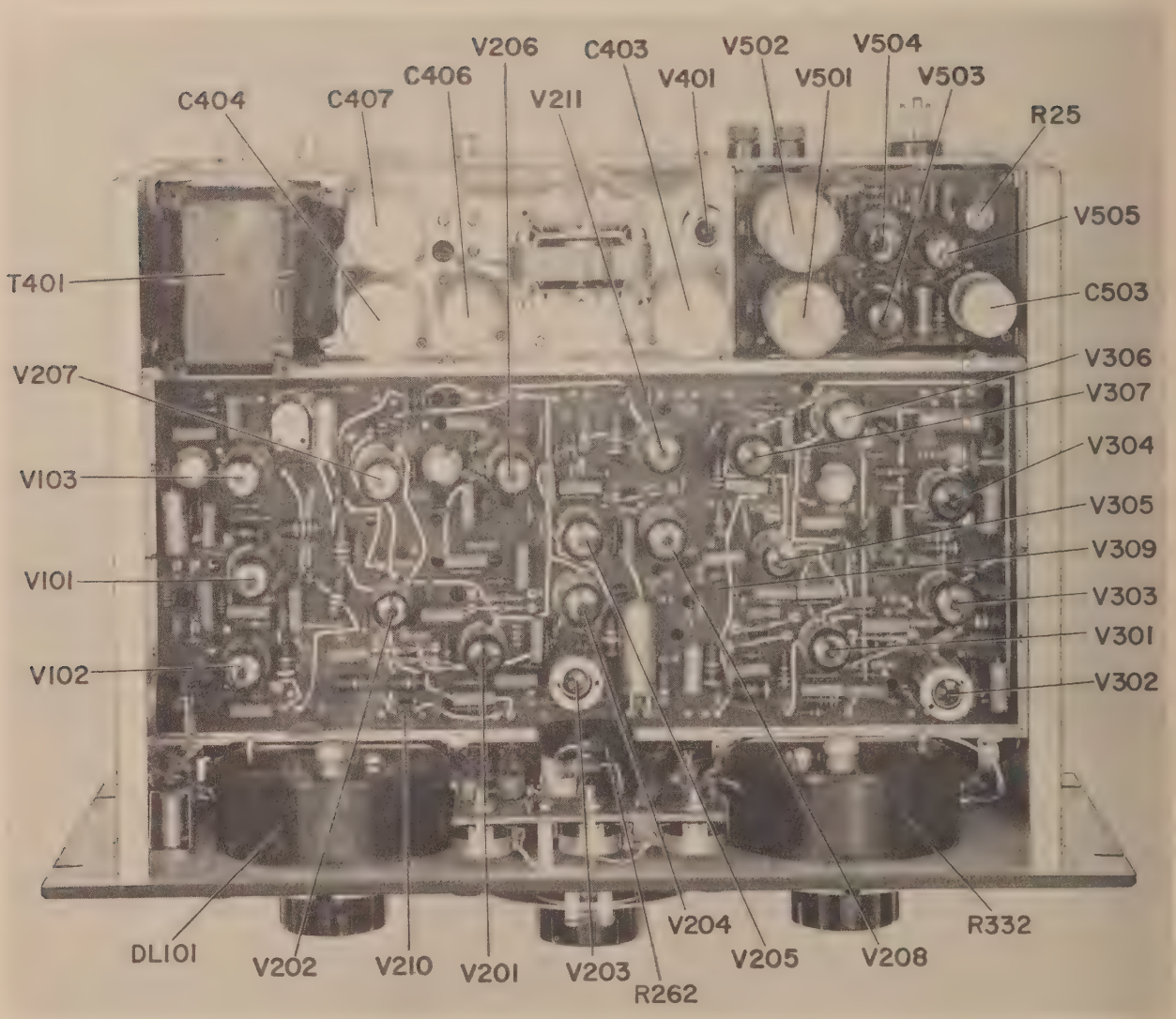
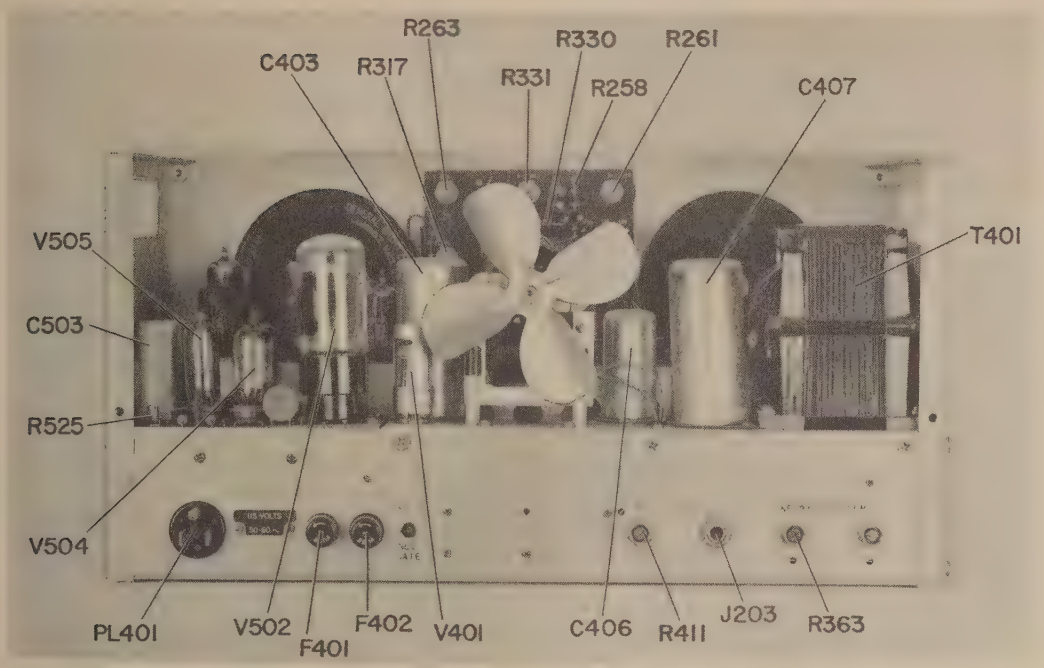
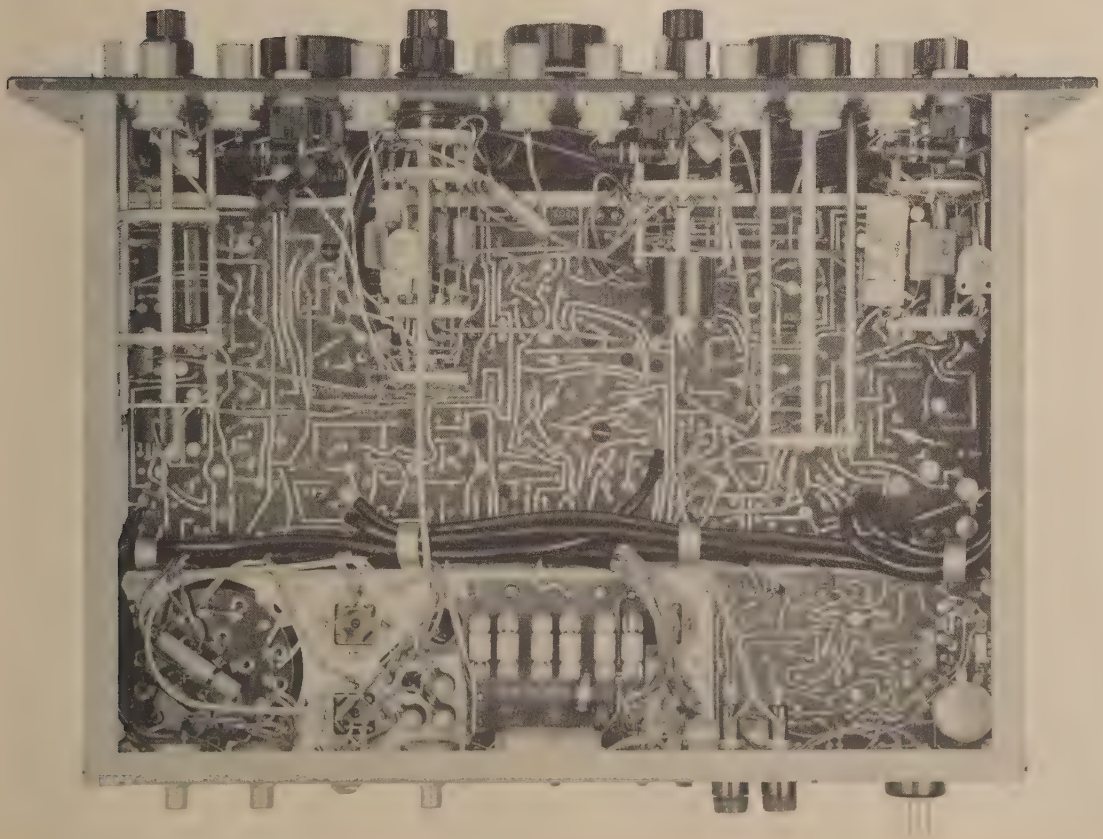


Figure 5.2. Top Interior View.
(Refer to Figure 5.5a for etched board layout.)

Figure 5.3. (Top, right) Rear Interior View.

Figure 5.4. (Bottom, right) Bottom Interior View.


R263
C403
R317
R330
R261
R331
R258
C407
V505
T401
C503
R525
V504
PL401
V502
F401
F402
V401
C406
R411
J203
R363



Section 6

PARTS LIST

RESISTORS. Resistance is in ohms unless otherwise indicated.

R101	51 k	±5%	1 w	REC-30BF
R102	33 k	±5%	1/2 w	REC-20BF
R103	510 k	±5%	1/2 w	REC-20BF
R106	1 k	±5%		971-410
R107	3.9 k	±10%	2 w	REC-41BF
R108	120 k	±5%	1/2 w	REC-20BF
R109	6.8 k	±5%	2 w	REC-41BF
R110	56 k	±5%	1/2 w	REC-20BF
R111	5.1 k	±5%	1 w	REC-30BF
R112	20 k	±5%	1/2 w	REC-20BF
R113	20 k	±5%	1/2 w	REC-20BF
R115	18 k	±5%	2 w	REC-41BF
R116	1 k	±5%	1 w	REC-30BF
R117	100	±5%	1/2 w	REC-20BF
R118	510	±5%	1/2 w	REC-20BF
R119	100	±5%	1/2 w	REC-20BF
R120	10	±5%	1/2 w	REC-20BF
R121	200 k	±5%	1/2 w	REC-20BF
R122	510	±5%	1/2 w	REC-20BF
R123	2.2 M	±50%	THYRITE	REU-8
R124	100	±5%	1/2 w	REC-20BF
R126	510	±5%	1/2 w	REC-20BF
R127	3 k	±5%	1/2 w	REC-20BF
R128	*	±5%	1/2 w	REC-20BF
R129	10	±5%	1/2 w	REC-20BF
R130	8.2 k	±5%	30 w	REPO-20P
R131	430	±5%	1/2 w	REC-20BF
R132	180	±5%	1/2 w	REC-20BF
R133	510	±5%	1/2 w	REC-20BF
R201	390	±5%	1/2 w	REC-20BF
R202	6.8 k	±10%	1 w	REC-30BF
R203	18 k	±5%	2 w	REC-41BF
R204	27 k	±10%	2 w	REC-41BF
R205	180 k	±5%	1/2 w	REC-20BF
R206	150 k	±5%	1/2 w	REC-20BF
R207	10 k	±5%	1/2 w	REC-20BF
R208	3.3 k	±5%	1 w	REC-30BF
R209	100 k	±1%	1/4 w	REF-65
R210	110 k	±1%	1/4 w	REF-65
R211	110 k	±1%	1/4 w	REF-65
R212	100 k	±1%	1/4 w	REF-65
R213	3.3 k	±5%	1 w	REC-30BF
R214	100 k	±5%	1/2 w	REC-20BF
R215	3 k	±10%	2 w	REC-41BF
R216	3 k	±10%	2 w	REC-41BF
R217	10 k	±5%	1/2 w	REC-20BF
R218	120 k	±5%	1/2 w	REC-20BF
R219	1.8 k	±10%	1 w	REC-30BF
R221	390 k	±1%	1/2 w	REF-70
R222	450 k	±1%	1/2 w	REF-70
R223	450 k	±1%	1/2 w	REF-70
R224	450 k	±1%	1/2 w	REF-70
R225	500 k	±1%	1/2 w	REF-70
R226	4.7 M	±1%	1 w	REF-75
R227	100 k	±20%		POSC-22
R228	100 k	±20%		POSC-22
R229	100 k	±20%		POSC-22
R230	100 k	±20%		POSC-22
R231	100 k	±20%		POSC-22
R232	1 M	±20%		POSC-22
R233	100	±5%	1/2 w	REC-20BF
R234	2.7 M	±5%	1/2 w	REC-20BF
R235	*	±5%	1/2 w	REC-20BF
R236	10 k	±5%	2 w	REC-41BF
R237	100	±5%	1/2 w	REC-20BF
R238	100	±5%	1/2 w	REC-20BF
R239	51	±5%	1/2 w	REC-20BF
R240	2.2 M	±50%	THYRITE	REU-8
R241	1.5 k	±5%	1/2 w	REC-20BF
R242	200 k	±5%	1/2 w	REC-20BF
R243	10	±5%	1/2 w	REC-20BF
R244	180	±5%	1/2 w	REC-20BF
R245	100	±5%	1/2 w	REC-20BF
R246	27 k	±5%	1 w	REC-30BF
R247	68 k	±5%	1/2 w	REC-20BF
R248	68 k	±5%	1/2 w	REC-20BF
R249	3 k	±5%	1/2 w	REC-20BF
R250	3 k	±5%	1/2 w	REC-20BF
R251	1 k	±10%	1 w	REC-30BF
R252	140 k	±1%	1/4 w	REF-65
R253	140 k	±1%	1/4 w	REF-65
R254	36 k	±5%	2 w	REC-41BF
R255	1 M	±5%	1/2 w	REC-20BF
R256	1 M	±5%	1/2 w	REC-20BF
R257	150 k	±5%	1/2 w	REC-20BF
R258	120 k	±5%	1/2 w	REC-20BF
R259	22 M	±5%	1/2 w	REC-20BF
R260	510 k	±5%	1/2 w	REC-20BF
R261	500	±10%		POSW-3
R262	10 k	±5%		1391-42
R263	5 k	±10%		POSW-3
R264	11 k	±10%	2 w	REC-41BF
R265	1 M	±5%	1/2 w	REC-20BF
R266	240 k	±5%	1/2 w	REC-20BF
R267	18 M	±5%	1/2 w	REC-20BF
R268	750	±5%	1/2 w	REC-20BF
R269	100	±5%	1/2 w	REC-20BF
R270	1.5 k	±5%	1/2 w	REC-20BF
R272	680	±5%	1/2 w	REC-20BF
R273	3 k	±5%	1/2 w	REC-20BF
R274	10	±5%	1/2 w	REC-20BF
R301	10 k	±5%	1/2 w	REC-20BF
R302	110 k	±1%	1/4 w	REF-65
R304	100 k	±1%	1/4 w	REF-65
R305	3.3 k	±5%	1 w	REC-30BF
R306	3 k	±10%	2 w	REC-41BF
R307	3 k	±10%	2 w	REC-41BF
R308	3.3 k	±5%	1 w	REC-30BF
R309	100 k	±5%	1/2 w	REC-20BF
R310	100 k	±1%	1/4 w	REF-65
R311	330 k	±5%	1/2 w	REC-20BF
R312	110 k	±1%	1/4 w	REF-65
R313	10 k	±5%	1/2 w	REC-20BF
R314	120 k	±5%	1/2 w	REC-20BF
R315	1.2 k	±10%	1 w	REC-30BF
R316	1 M	±5%	1/2 w	REC-20BF
R317	100 k	±10%		POSC-11

5.4.5 DIRECT SYNC, DELAY NO. 2 SYNC PRESENT; DELAY NO. 1 GATE AND SYNC ABSENT. Defect is on Delay No. 1 circuits. Throw the DELAY LINE FUNCTION switch to the 0-1-μsec position. If the sync is still absent, refer to paragraph 5.4.5.1. If the sync is present, refer to paragraph 5.4.5.2.

5.4.5.1 No. 1 Sync Absent with DELAY LINE FUNCTION Switch in Either VERNIER or 0-1-μsec Position.

a. Set the DELAY LINE FUNCTION switch to the DELAY No. 2 SYNC position. If the Delay No. 1 monitor light comes on, then the defect must be in the delay line itself or in its wiring or switching.

b. If the No. 1 sync pulse is still absent, then the defective tube or component must be associated with V206 or V207. Check waveforms at TP204, TP205, and check voltages and components associated with these stages.

5.4.5.2 No. 1 Sync Absent With DELAY LINE FUNCTION Switch in VERNIER Position, Present With Switch in 0-1-μsec Position. Placing the DELAY LINE FUNCTION switch in 0-1-μsec position and establishing the fact that the instrument operates eliminates V206 and V207. The difficulty must lie in the gate, sweep generator, or amplitude comparator. Proceed as follows:

a. Remove the cover of the instrument.

b. Observe the Delay No. 1 automatic reset lamp (V210) with the prf drive (10 kc) applied. If the bulb flashes intermittently, proceed to (1) below. If not, refer to (2).

(1) Delay No. 1 automatic reset bulb flashing: This indicates that the sweep voltage is high. The sweep generator tube, V203, is off, the right-hand tube of the gate is on, and the amplitude comparator is set into "active state" and will be stable in this position. The trouble may be the amplitude comparator V205, V202, V211, the sweep generator V203, or the bistable gate V201. The possibility that V206 is weak should not be overlooked, since the signal at its cathode in the 0-1-μsec range is larger than its grid drive. Test point waveforms are of little use in locating this trouble. A systematic replacement of tubes with tubes known to be functioning (exchange with Delay No. 2) and then a check of voltages against Table 5 is the best procedure.

(2) Delay No. 1 automatic reset lamp not flashing. This indicates that the sweep voltage is never rising. Beyond some possibility of a grid-cathode short in V208, the amplitude comparator is eliminated. Most likely source of trouble is V201. Check V201 by substitution. Check D201 and D203. Check V203 (turn instrument OFF before unplugging V203). Check D205 for an open circuit. If these actions do not help, check the d-c voltages on V201 and V203 against Table 5.

5.4.6 DIRECT SYNC, DELAY NO. 1 SYNC, AND DELAY NO. 2 SYNC AND GATE PRESENT. DELAY NO. 1 GATE ABSENT. Only the gate amplifier tube, V202, is involved. Check this tube. If it is all right, check its associated components.

5.4.7 DIRECT SYNC, NO. 1 GATE AND SYNC, NO. 2 SYNC ALL PRESENT. NO. 2 GATE MISSING. If the COINC SENSITIVITY control is fully clockwise and the panel fitting is not damaged and short-circuiting, then V305 or one of its associated components is defective. Check the tube and its components.

5.4.8 DIRECT SYNC, NO. 1 GATE AND SYNC, NO. 2 GATE PRESENT. NO. 2 SYNC MISSING. The only tube not directly involved in the delay and resetting circuit for the No. 2 delay is the sync blocking oscillator. Check V306 and its components. Make sure that the coaxial connector has not been damaged.

5.4.9 DIRECT SYNC, DELAY NO. 1 SYNC, AND GATE ALL PRESENT. DELAY NO. 2 SYNC AND GATE ABSENT. This set of symptoms indicates a failure somewhere in the delay loop. There are two types of failure immediately recognizable. Remove instrument cover. If the Delay No. 2 automatic reset lamp is flashing, refer to (1) below. If it is not flashing, refer to (2).

(1) Delay No. 2 Automatic Reset Lamp Flashing. This indicates that V302, the sweep generator tube, is off and the sweep voltage is high. The amplitude comparator has not reset the gate. The gate itself is probably all right. If the reset bulb stops flashing when the prf drive is removed, the gate and V302 almost certainly are all right and need not be tested. First check V302, V304, and V303 by replacement with tubes known to be good and then check their electrode voltages. If light continues to flash even when there is no drive, check V301 and V302.

(2) Delay No. 2 Automatic Reset Lamp, V309, Not Flashing. These symptoms show that the sweep voltage at the grid of V304 never rises. Either the gate never opens V302, or the triode section of V303 is defective. First check these tubes. If they are all right, check the diodes in gate circuits. Then check the gate d-c voltages (Table 5).

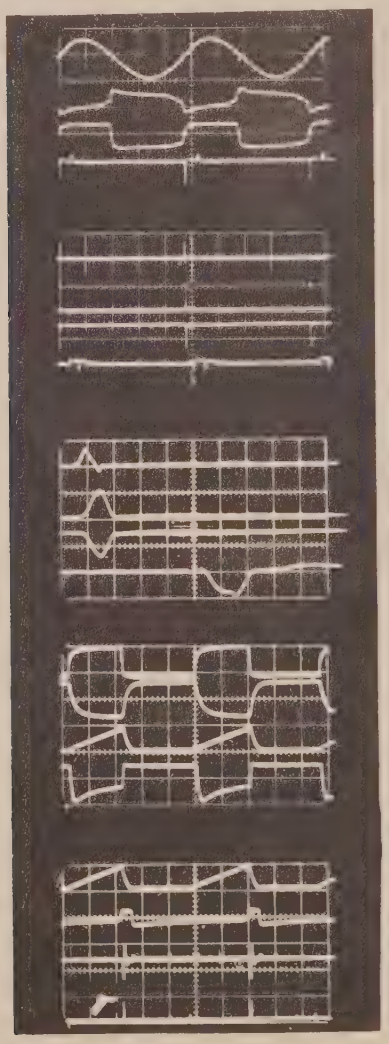
5.4.10 ALL OUTPUTS NORMAL, NO COINCIDENCE PULSES APPEAR ON COINCIDENCE GATE, PULSE INPUT PRESENT AT COINCIDENCE DRIVE TERMINALS. The only stage involved is V307. Check this tube and its associated components.

5.4.11 EITHER SYNC MONITOR LAMP GLOWS CONTINUOUSLY, WHETHER OR NOT SYNC IS PRESENT. The only possibility is the monitor amplifier. Check and, if necessary, replace V307 and V206.

5.4.12 EITHER SYNC MONITOR LAMP FAILS TO LIGHT WHEN SYNC IS PRESENT. Again, difficulty is probably associated with amplifier tube, V307, or with V206. If a new tube fails to remedy the difficulty, check components from the input coupling capacitor of these stages onward.

5.5 TROUBLE-SHOOTING IN POWER SUPPLIES.

5.5.1 GENERAL. Power-supply trouble-shooting is straightforward. It is complicated only slightly by the presence of the vacuum-tube regulator circuits. These regulators will hold their output voltage for a time as rectifiers or filters deteriorate, but then will fail first at low line input when all of their reliability margins are used up. If the output of a power supply is low, first check the unregulated input voltage (115-volt line) against the nominal value listed on page 24. If the input voltage is normal, then the regulator circuit can be checked by tube replacement or voltage measurements. Higher-than-normal output voltage probably indicates a defective series-regulator tube or a defective amplifier tube in VR401. Excessive hum or noise on the +250-volt regulated bus probably indicates a defective amplifier tube in VR401, and these tubes should be checked. The most critical tube in this respect is probably V503.



1. PRF 100 KC, WRITING RATE 2μSEC/CM.
   A. INPUT SIGNAL, 5V/CM
   B. TP101 50V/CM
   C. TP102 50V/CM
   D. TP103 50V/CM

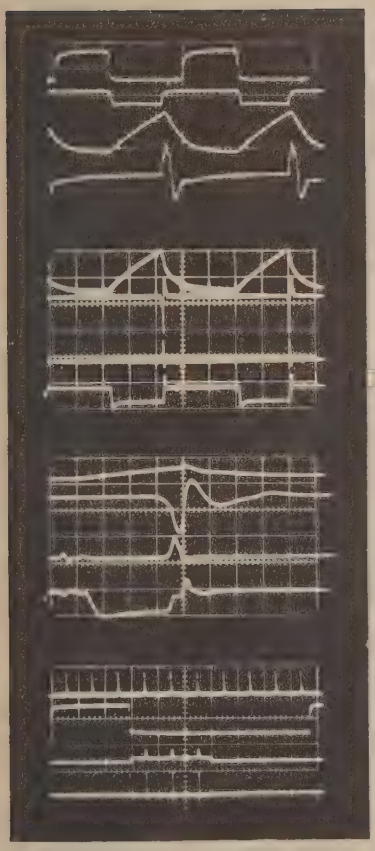
2. PRF 100 KC, WRITING RATE 2μSEC/CM, 0.5-μSEC DELAY.
   A. TP104 20V/CM
   B. POS DIRECT SYNC 20V/CM
   C. NEG DIRECT SYNC 20V/CM
   D. PIN 7 V206 (S202, 109R) 10V/CM

3. PRF 100 KC, WRITING RATE 0.1 μSEC/CM, 0.5-μSEC DELAY.
   A. TP104 20V/CM
   B. POS DIRECT SYNC 20V/CM
   C. NEG DIRECT SYNC 20V/CM
   D. PIN 7 V206 (S202, 109R) 10V/CM

4.
   A. POS DELAY NO. 1 GATE 5V/CM
   B. NEG DELAY NO. 1 GATE (4 μSEC DELAY) 5V/CM
   C. TP202 50V/CM
   D. TP201 20V/CM

5.
   A. TP202 50V/CM
   B. TP203 20V/CM
   C. TP204 200V/CM
   D. TP205 10V/CM

Figure 5.1. Test Waveforms for Trouble-Shooting.



6. DELAY NO. 1, 4 μSEC; DELAY NO. 2, 4 μSEC.
   A. POS GATE, DELAY NO. 2 5V/CM
   B. TP301 20V/CM
   C. TP302 50V/CM
   D. TP303 5V/CM

7. DELAY NO. 1, 4 μSEC; DELAY NO. 2, 4 μSEC.
   A. TP302 50V/CM
   B. TP304 10V/CM
   C. TP306 10V/CM
   D. TP305 5V/CM

8. DELAY NO. 1, 0.1 μSEC; DELAY NO. 2, 0.7 μSEC. 0.2 μSEC/CM.
   A. TP302 50V/CM
   B. TP304 100V/CM
   C. TP306 100V/CM
   D. TP305 10V/CM

9. PRF 10 KC, DELAY NO. 1 35 μSEC, DELAY NO. 2 30 μSEC.
   (Set DELAY LINE FUNCTION switch to VERNIER and DELAY NO. 2 FUNCTION switch to COINC DRIVE.)
   A. 10-μSEC PULSES FROM 180-A TO POS COINC, 10V/CM
   B. 30-μSEC DELAY NO. 1 GATE, 5V/CM
   C. 30-μSEC DELAY NO. 2 GATE, 5V/CM
   D. TP305 100V/CM

Figure 5.1. Test Waveforms for Trouble-Shooting. (Continued)

TABLE OF VOLTAGES AND RESISTANCES

TUBE (TYPE)	PIN	DC VOLTS		RES TO GND
		TRIG LEVEL CCW	TRIG LEVEL CW	
V101 (6U8)	1	+106	+40	51 k
	2	-5.9	-5.8	10 k
	3	+228	+228	18 k
	6	+245	+245	1.1 k
	8	+2.7	0	1 k
	9	0	-0.2	2 k
V102 (6BQ7)	1	+190	+245	3.9 k
	2	+106	+40.5	54.5 k
	3	+106	+77	6.8 k
	6	+250	+197	5.1 k
	7	+58	+75	56 k
	8	+106	+77	6.8 k
V103 (6350)	1	+245	+245	1.5 k
	2	-21	-21	30
	3	-39	-39	35 k
	6	+245	+245	1.1 k
	7	-21	-21	130
	8	-39	-39	35 k
V201 (5965)	1	+104		8 k
	2	-0.45		2.5 k
	3	0		0
	6	+140		8 k
	7	-12.3		2.5 k
	8	0		0
V202 (6AU6)	1	-12		85 k
	2	0		390
	5	+250		6.8 k
	6	+150		10.8 k
	7	0		390
V203 (12AT7)	1	+17		540 k
	2	0		60 k
	3	0		0
	4	0		0
	5	-12		11
	6	+17.5		1.8 k
	7	+17.5		1.8 k
	8	+17		540 k
V204 (5965)	1	+250		0
	2	+17.3		510 k
	3	+22.5		10 k
	6	+22.5		10 k
	7	-0.7		2.7 M
	8	0		100
V205 (5965)	1	+250		3 k
	2	+195		32 k
	3	+205		37.5 k
	6	+235		3 k
	7	+205		143 k
	8	+205		37.5 k

TUBE (TYPE)	PIN	DC VOLTS	RES TO GND
V206 (6U8)	1	+17.5	240 k
	2	-6	34 k
	3	+13.5	30.5 k
	6	+250	1.1 k
	7	+13.5	
	8	-21.8	22
	9	-21	18 M
V207 (6350)	1	+250	1.1 k
	2	-24	130
	3	-43.5	135 k
	6	+250	1.18 k
	7	-24	32
	8	-43.5	135 k
V208 (5751)	1	+195	32 k
	2	+27	515 k
	3	+29	
	4	-24	11
	5	-12	11
	6	+205	143 k
	7	+17	540 k
	8	+30	
V211 (5751)	1	+30	
	2	-75	500 k
	3	-74	150 k
V301 (5965)	1	+103	8 k
	2	-0.4	2.5 k
	3	0	0
	6	+140	8 k
	7	-12.3	2.5 k
	8	0	0
V302 (12AT7)	1	+19.2	210 k
	2	0	60 k
	3	0	0
	6	+12	1.2 k
	7	+12	1.2 k
	8	+19.3	210 k
V303 (6AU8)	1	+26	15 k
	2	+19	215 k
	3	+250	0
	6	+6	1 k
	7	0	33 k
	8	+160	82 k
	9	242	5 k
V304 (12AX7)	1	+223	47 k
	2	+26	15 k
	3	+39	9 k
	6	+240	5.6 k
	7	+38	28 k
	8	+39	9 k

PARTS LIST (Cont)

RECTIFIERS	
RX401	1N1695
RX402	1N1695
RX403	1N1695
RX404	1N1695
RX405	1N1695
RX406	1N1695

TUBES	
V101	6U8
V102	6BQ7A
V103	6350
V201	5965
V202	6AU6
V203	1392-12AT7
V204	5965
V205	5965
V206	6U8
V207	6350
V208	5751
V209	SOL-12 (NE-2A)
V210	NE-2
V211	5751
V301	5965
V302	1392-12AT7
V303	6AU8A
V304	12AX7
V305	6485
V306	6350
V307	5965
V308	SOL-12 (NE-2A)
V309	NE-2
V401	6AU6
V402	NE-2
V403	NE-2
V404	NE-2
V501	6AV5GA
V502	6AV5GA
V503	6AN8
V504	5965
V505	5651

MISCELLANEOUS	
BL401	BLOWER, 1392-306
DL101	DELAY LINE, 1477-J1000-400
L101	CHOKE, 120 μh ±10% CHM-3
L301	CHOKE, 1 mh CHA-3
P401	PILOT LAMP, 6.3 v Mazda #44 2LAP-939
PL401	PLUG CDPP-10
VR401	VOLTAGE REGULATOR 1200-402-250

NOTES

* - Value determined at General Radio laboratory.
** - May be padded at General Radio laboratory.

Type designations for resistors and capacitors are as follows:

COC - Capacitor, ceramic
COE - Capacitor, electrolytic
COL - Capacitor, oil
COM - Capacitor, mica
COP - Capacitor, plastic
COT - Capacitor, trimmer
COW - Capacitor, wax
POSC - Potentiometer, composition
POSW - Potentiometer, wire-wound
REC - Resistor, composition
REF - Resistor, film
REPO - Resistor, power
REU - Resistor, unclassified
REW - Resistor, wire-wound

When ordering replacement components, be sure to include complete description as well as Part Number. (Example: R85, 51K ±10%, 1/2w, REC-20BF).

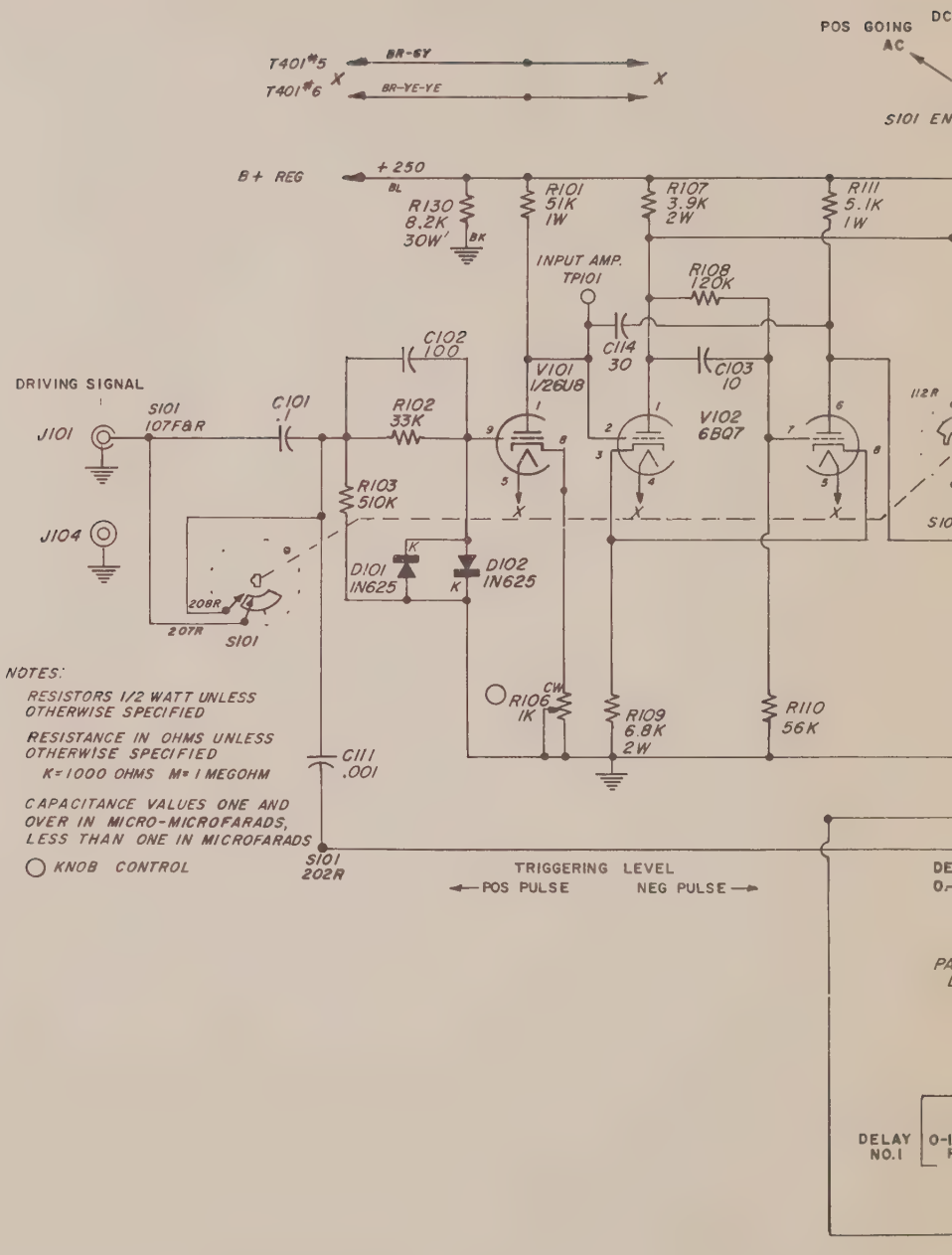
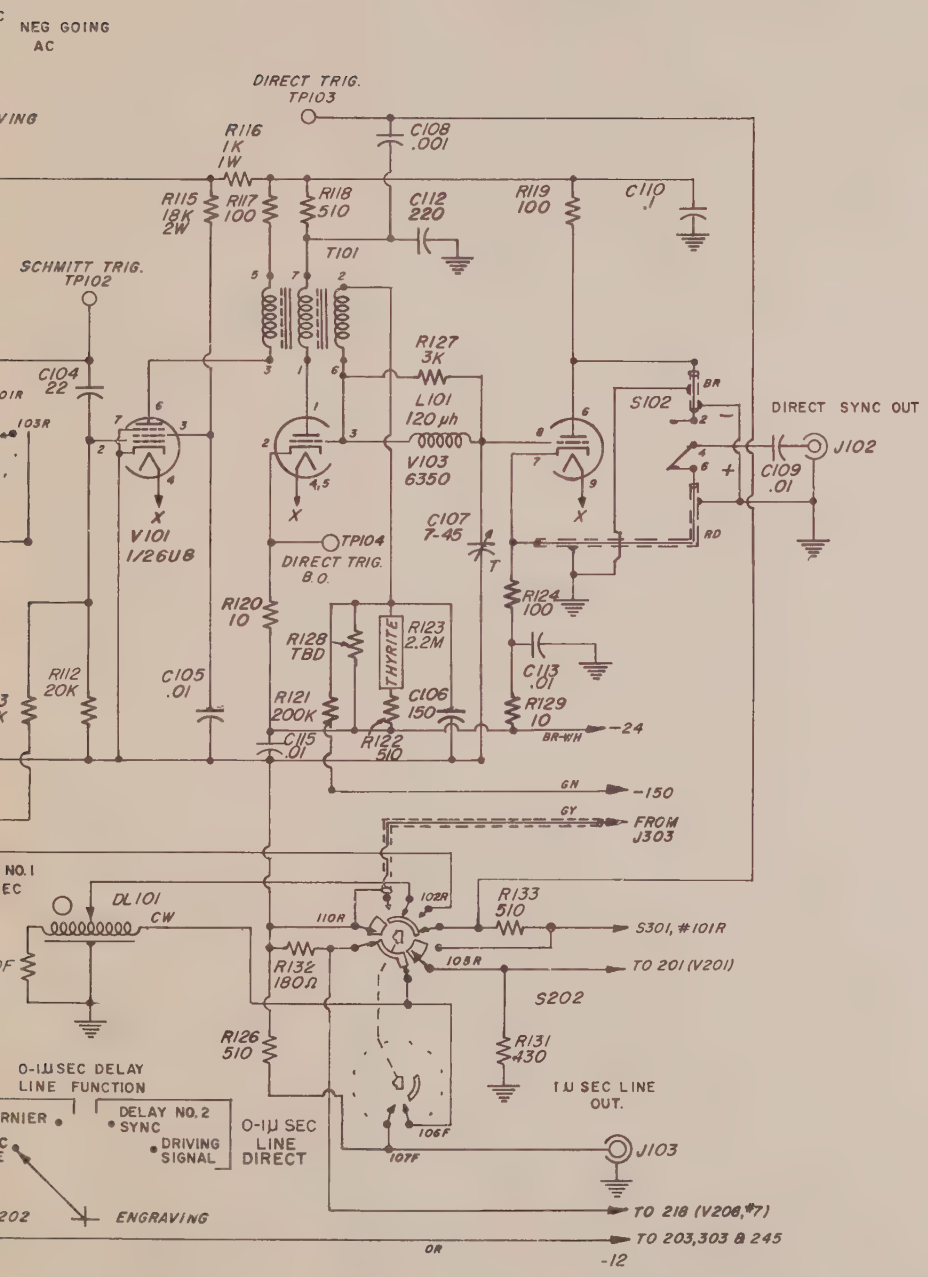
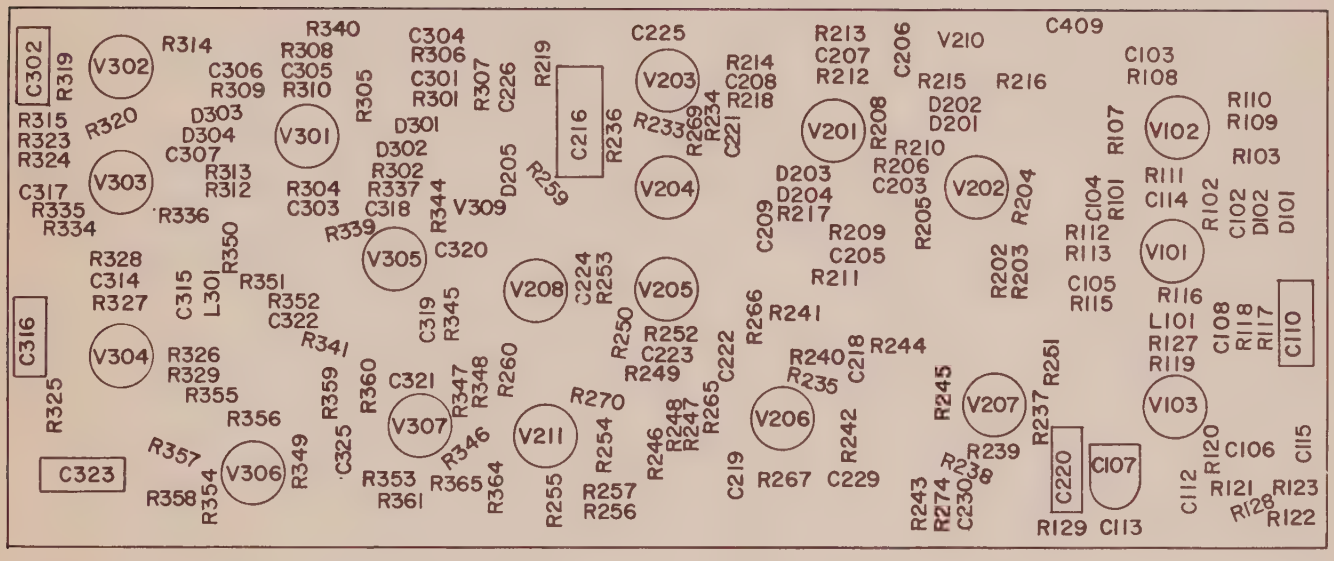


Figure 5.5. Schematic D



am, Input Circuits.


C302
R319
V302
R314
R340
R308
C305
R310
C304
R306
C301
R301
C306
R309
R305
R307
C226
R219
C225
V203
R214
C208
R218
C216
R236
R233
R269
R234
C221
V201
R208
C206
V210
C409
C103
R108
R213
C207
R212
R215
R216
D202
D201
R210
R206
C203
V202
R204
R107
V102
R110
R109
R103
R111
C114
C104
R101
R102
C102
D102
D101
R112
R113
V101
R116
C105
R115
R202
R203
C108
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C110
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R219

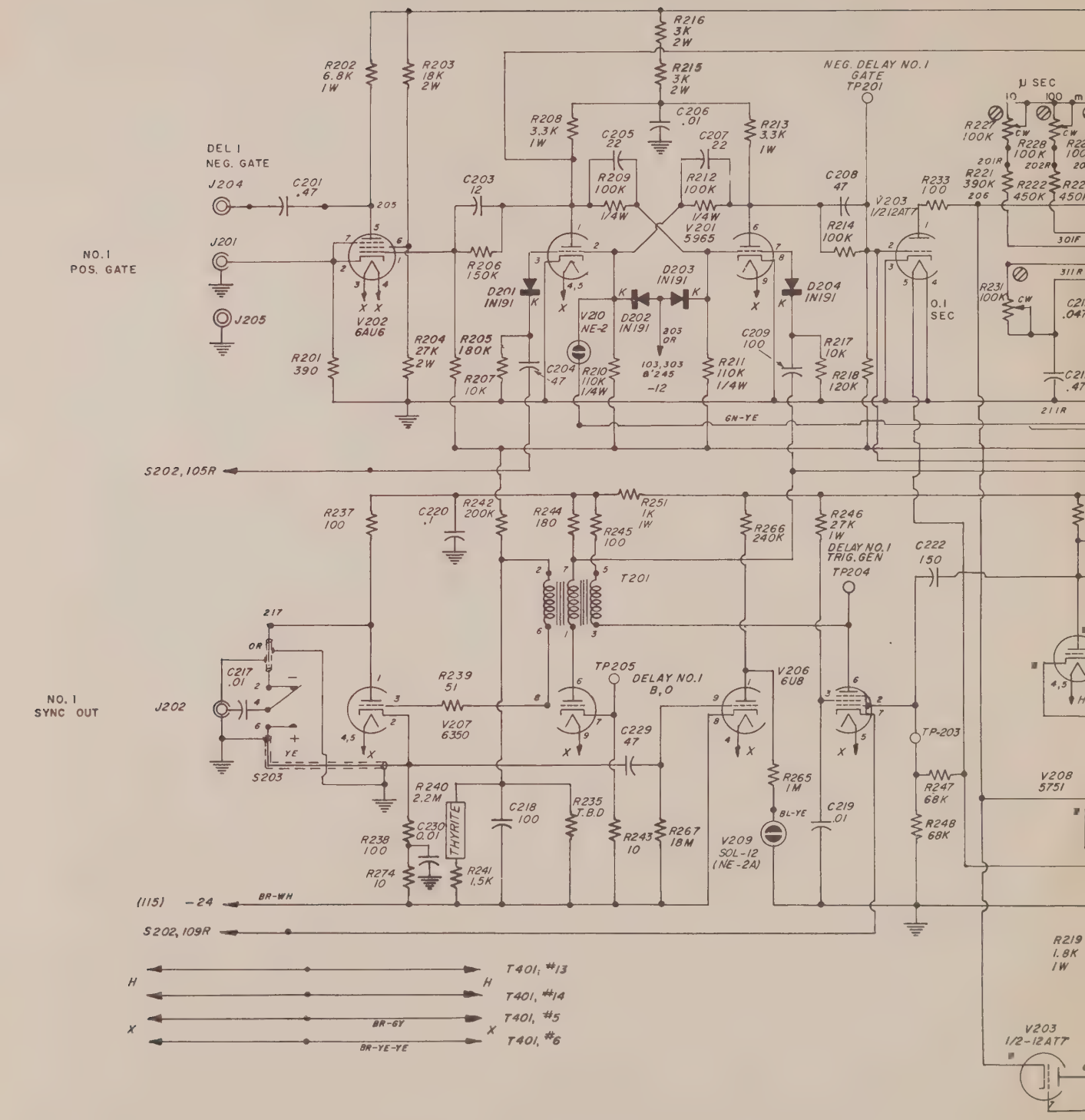
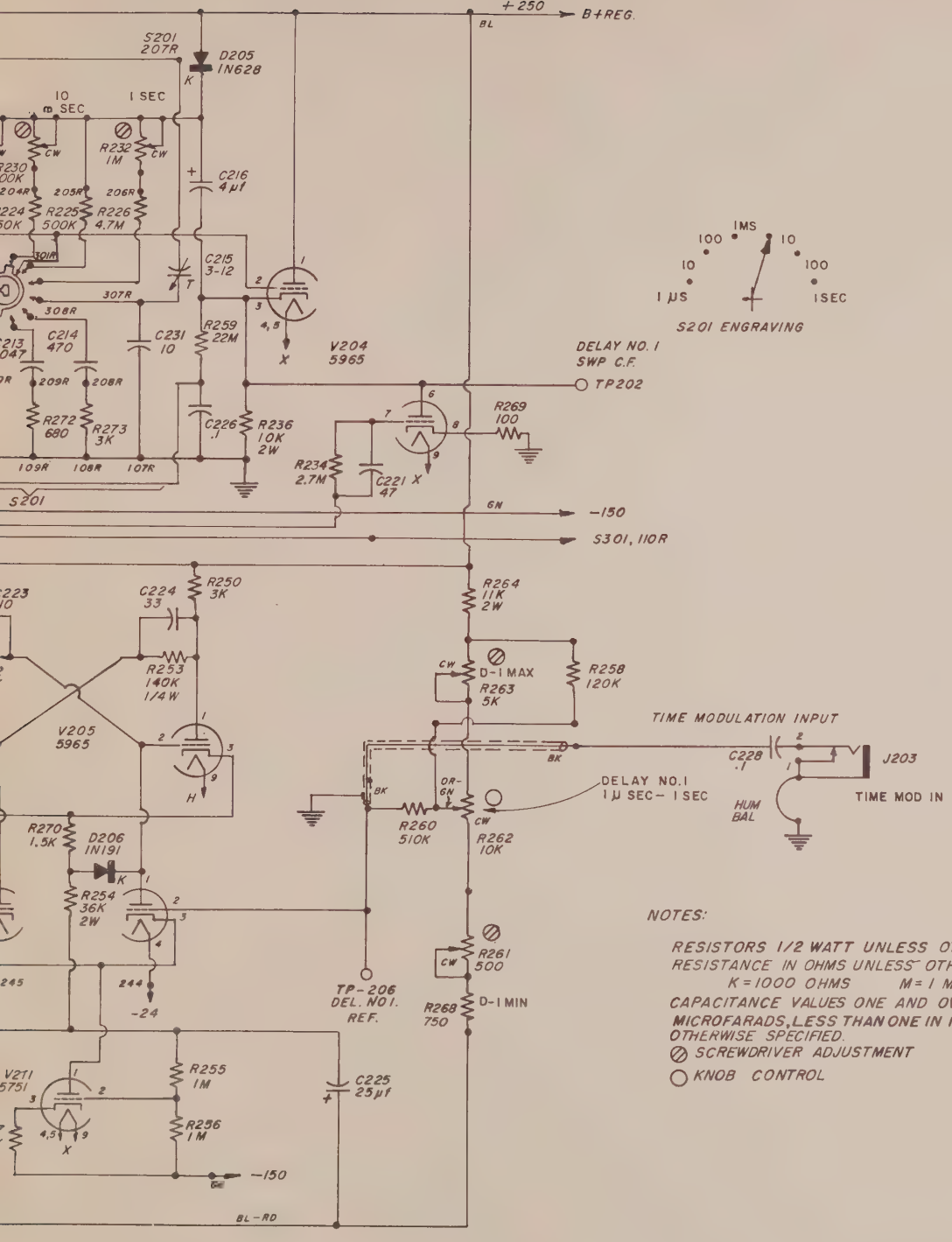


Figure 5.6. Schematic Dia



NOTES:

RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED
RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K = 1000 OHMS M = 1 MEGOHM
CAPACITANCE VALUES ONE AND OVER IN MICRO MICROFARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
⊘ SCREWDRIVER ADJUSTMENT
◯ KNOB CONTROL

. Delay No. 1 Circuits.

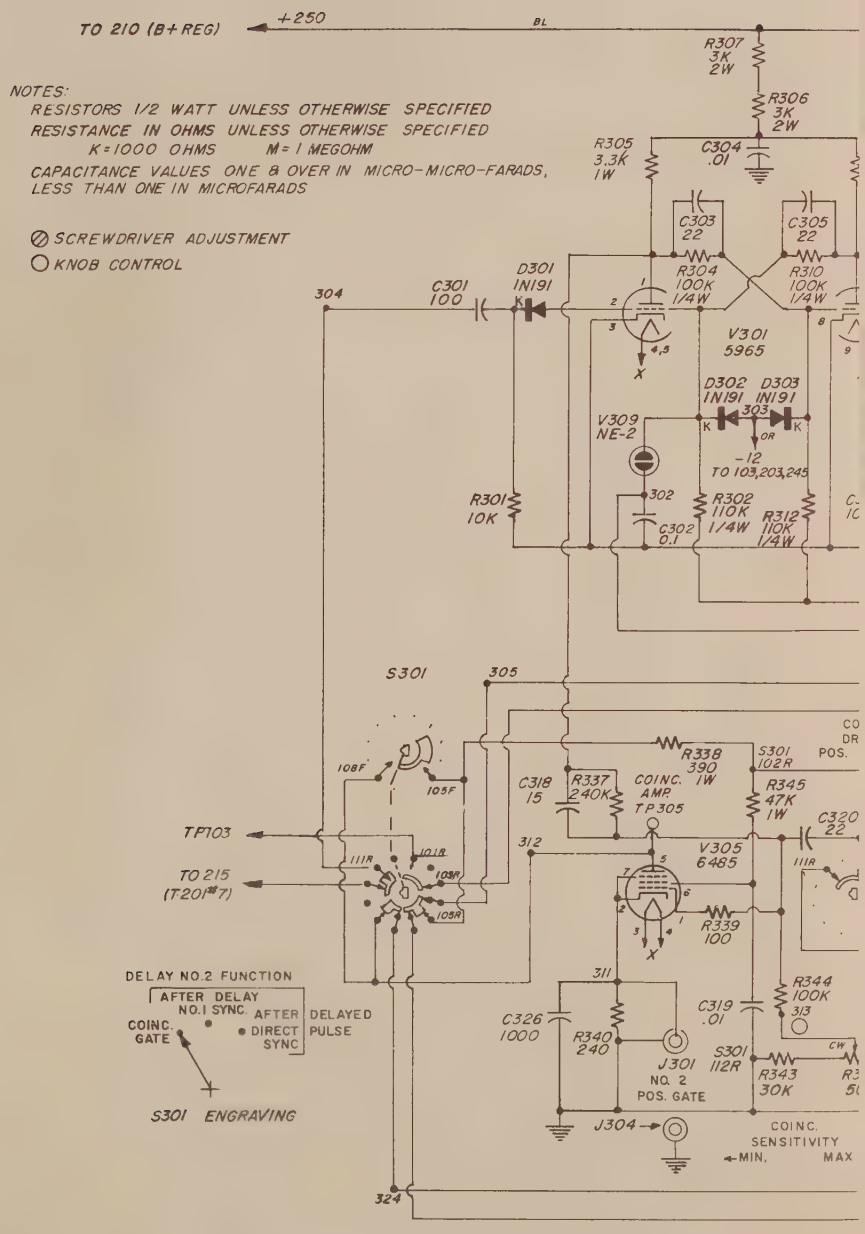
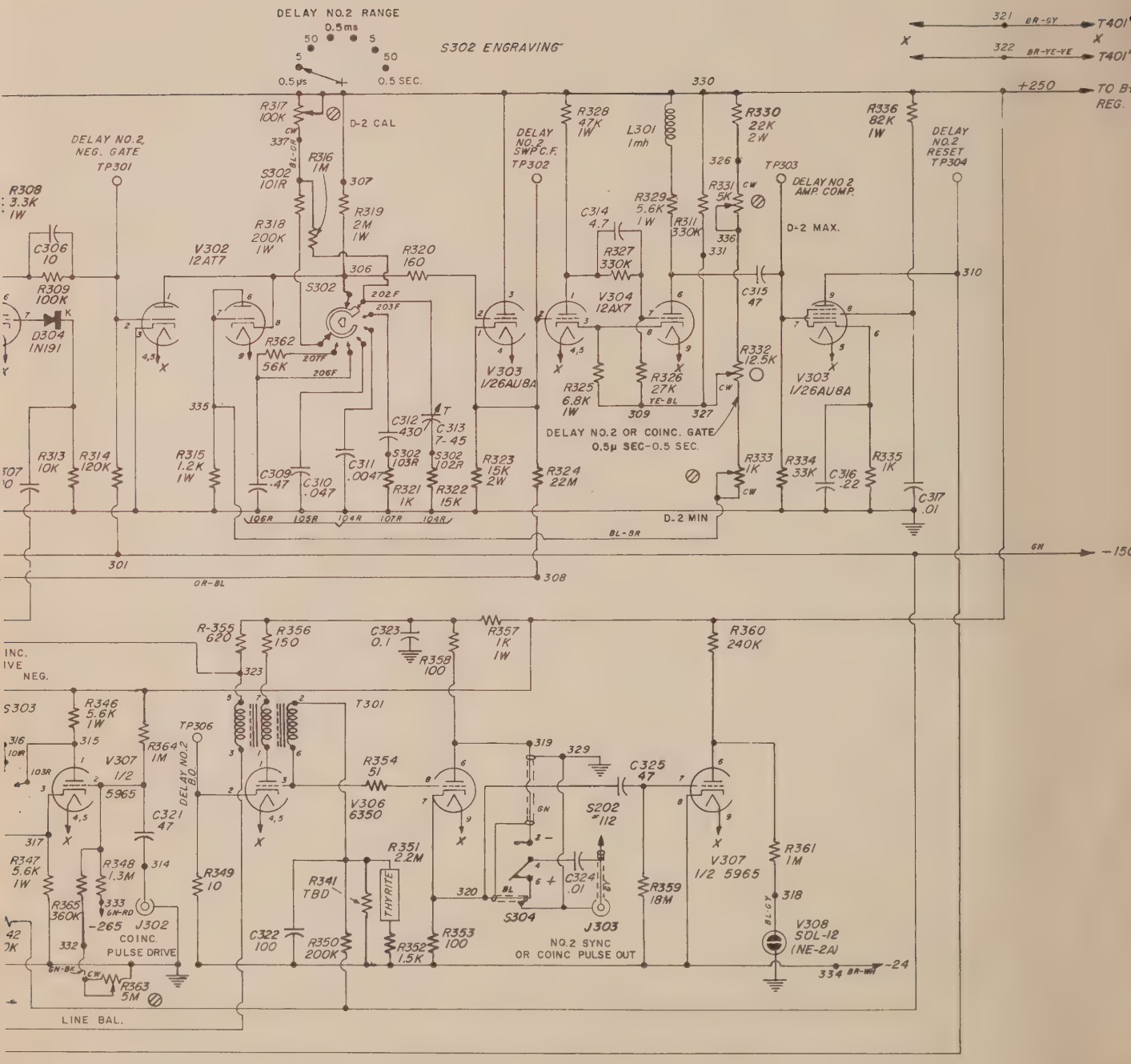
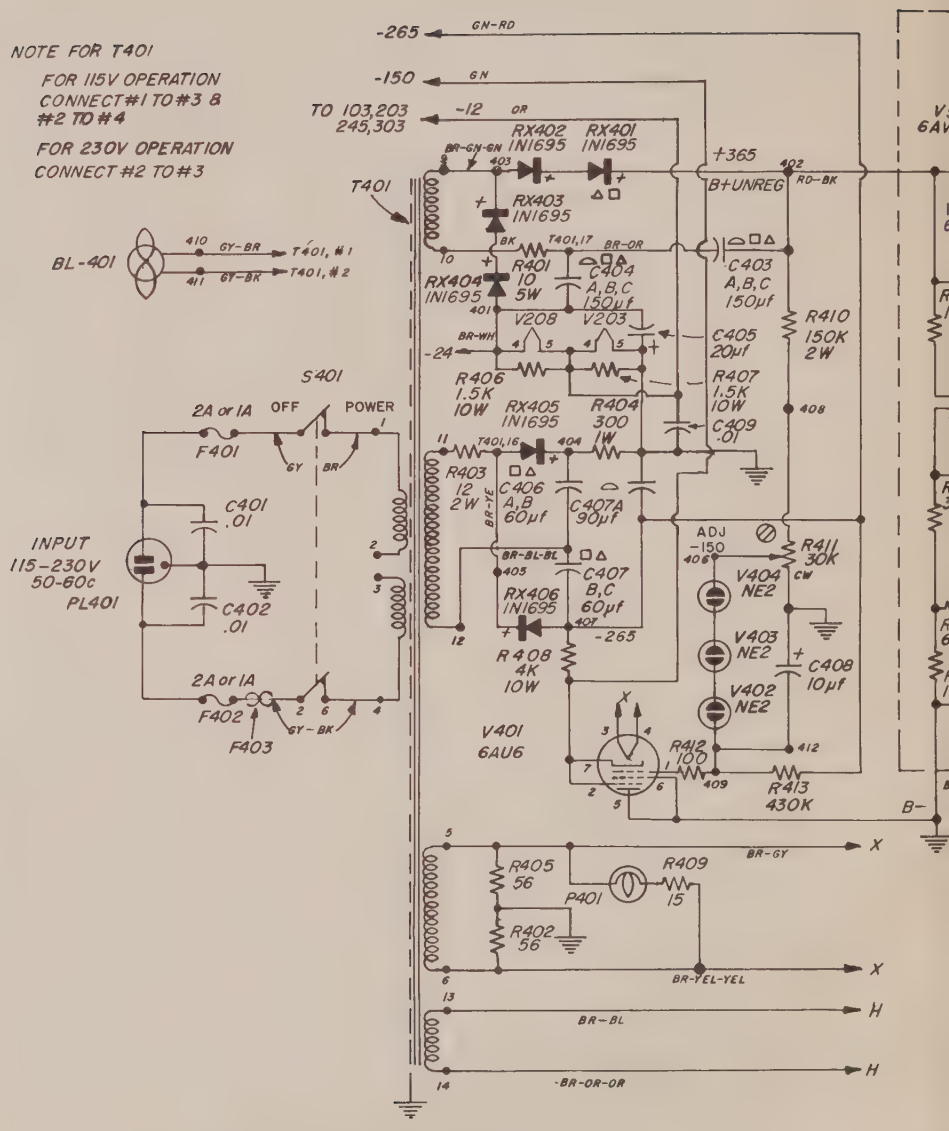


Figure 5.7. Schematic D



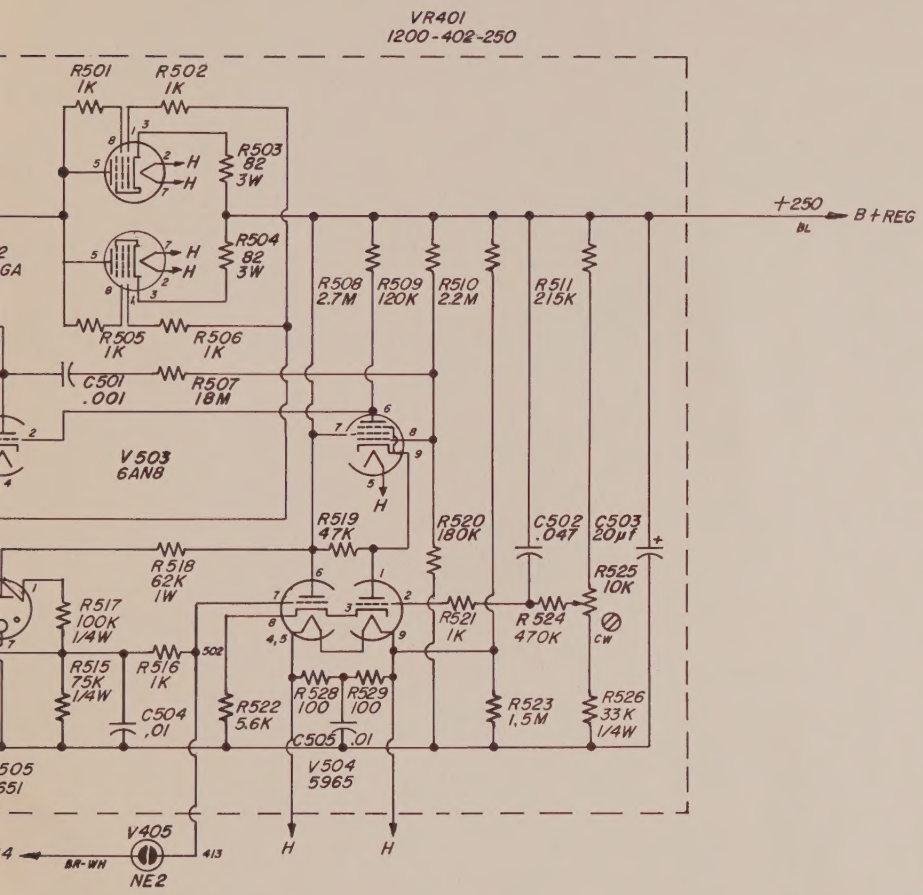
iagram, Delay No. 2 Circuits.



NOTES:
RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED
RESISTANCE IN OHMS UNLESS OTHERWISE SPECIFIED
K=1000 OHMS M=1 MEGOHM
CAPACITANCE VALUES ONE AND OVER IN MICRO MICROFARADS, LESS THAN ONE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.

⊘ SCREWDRIVER ADJUSTMENT

Figure 5.8. Schematic D



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